

Intel Calpella Platform – K52JT

- Calpella Platform Block Diagram
- Ibex Peak-M Overview
- K52JT Architecture
- [Repair reference] - No power
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- [Repair reference] - Vcore Problems
- [Repair reference] - Battery Charging problems
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- [Repair reference] - Audio problems
- Q & A

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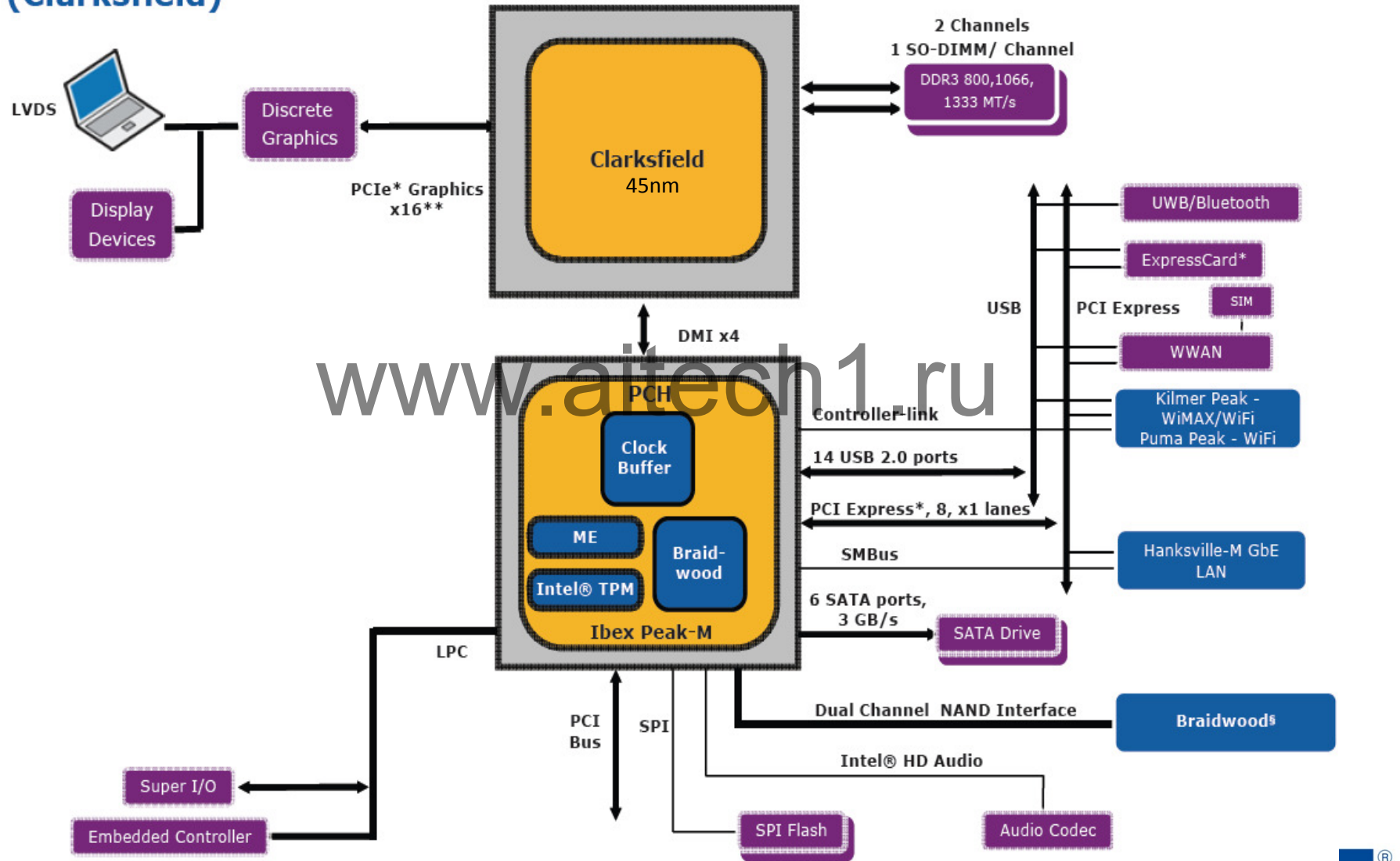
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(Auburndale)



Calpella platform

(Clarksfield)



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Calpella PCH

**14 USB ports with
USB2.0 Rate
Matching Hub**

**6 SATA ports with
Port Multiplier
Support & FIS Based
Switching**

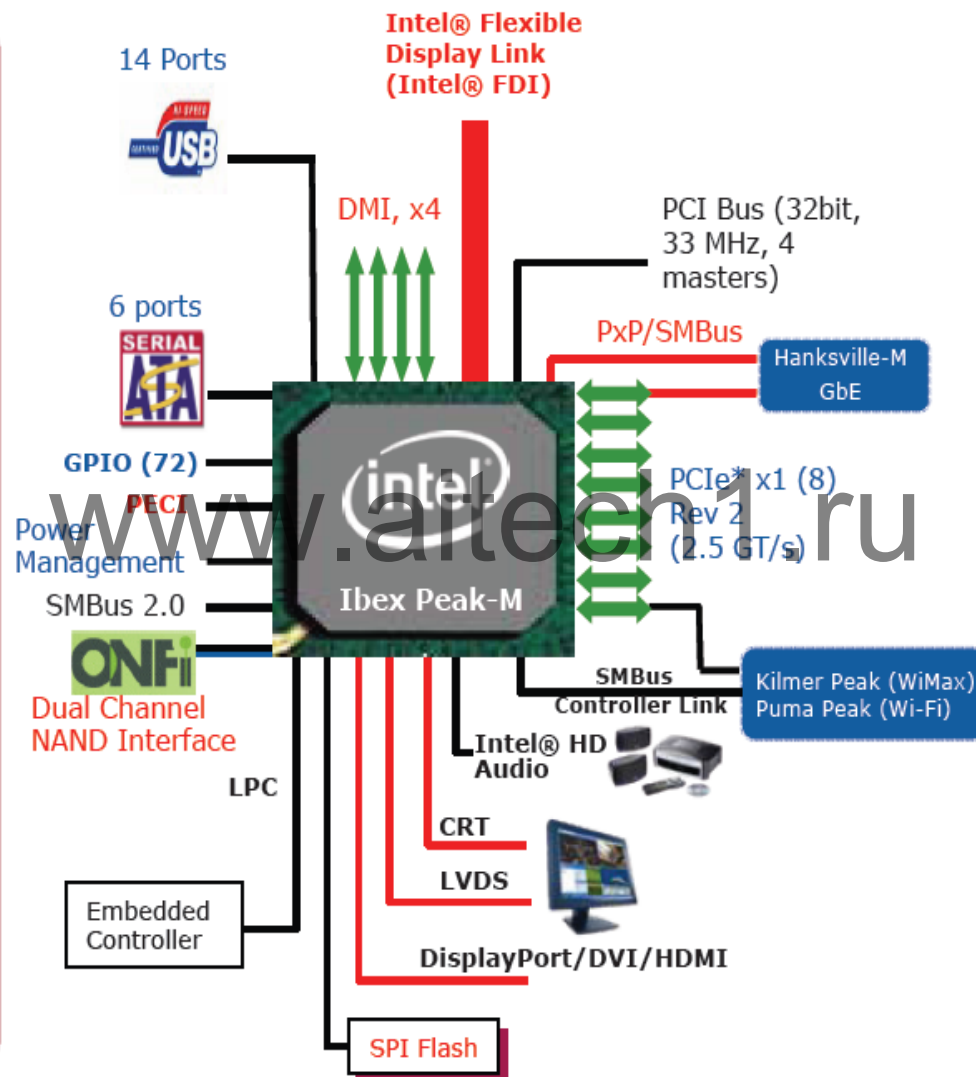
**Support for eSATA
Port, Command
Based PM support**

**8 PCIe* ports – 2
more than in
previous platform**

1.1-V Core Voltage

**PECI and Thermal
Management support**

**Intel® VT-d
Virtualized I/O
Support**



**Integrated MAC w/
LinkSec
(802.1AE, 802.1AF)**

**Integrated NVRAM
Controller with Fast
Flash support**

**Integrated
Manageability Engine**

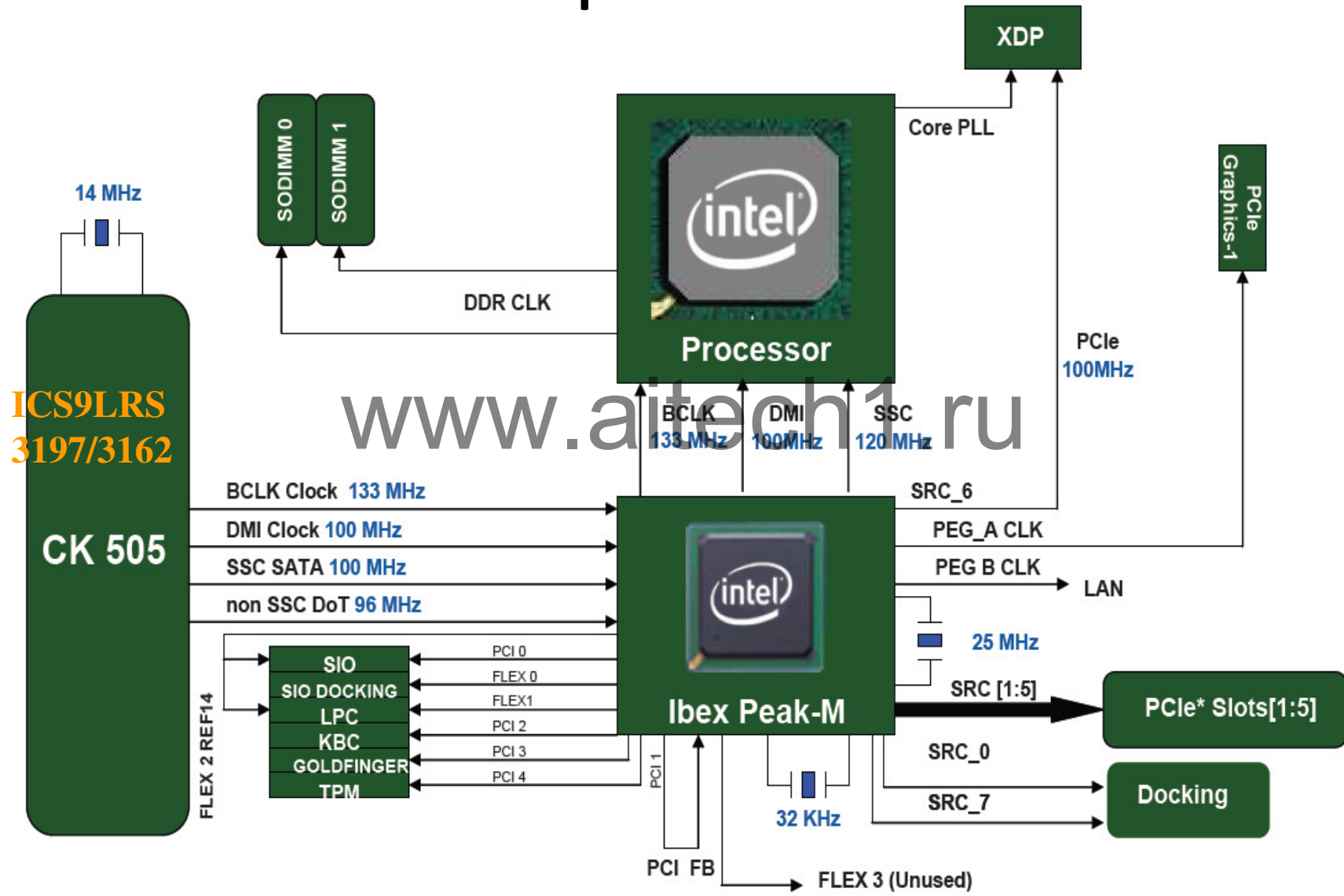
**Integrated TPM
support**

**Intel® Anti-theft
Technology**

Buffered Clocking

**Display Interfaces
and Intel® FDI**

Calpella CLK

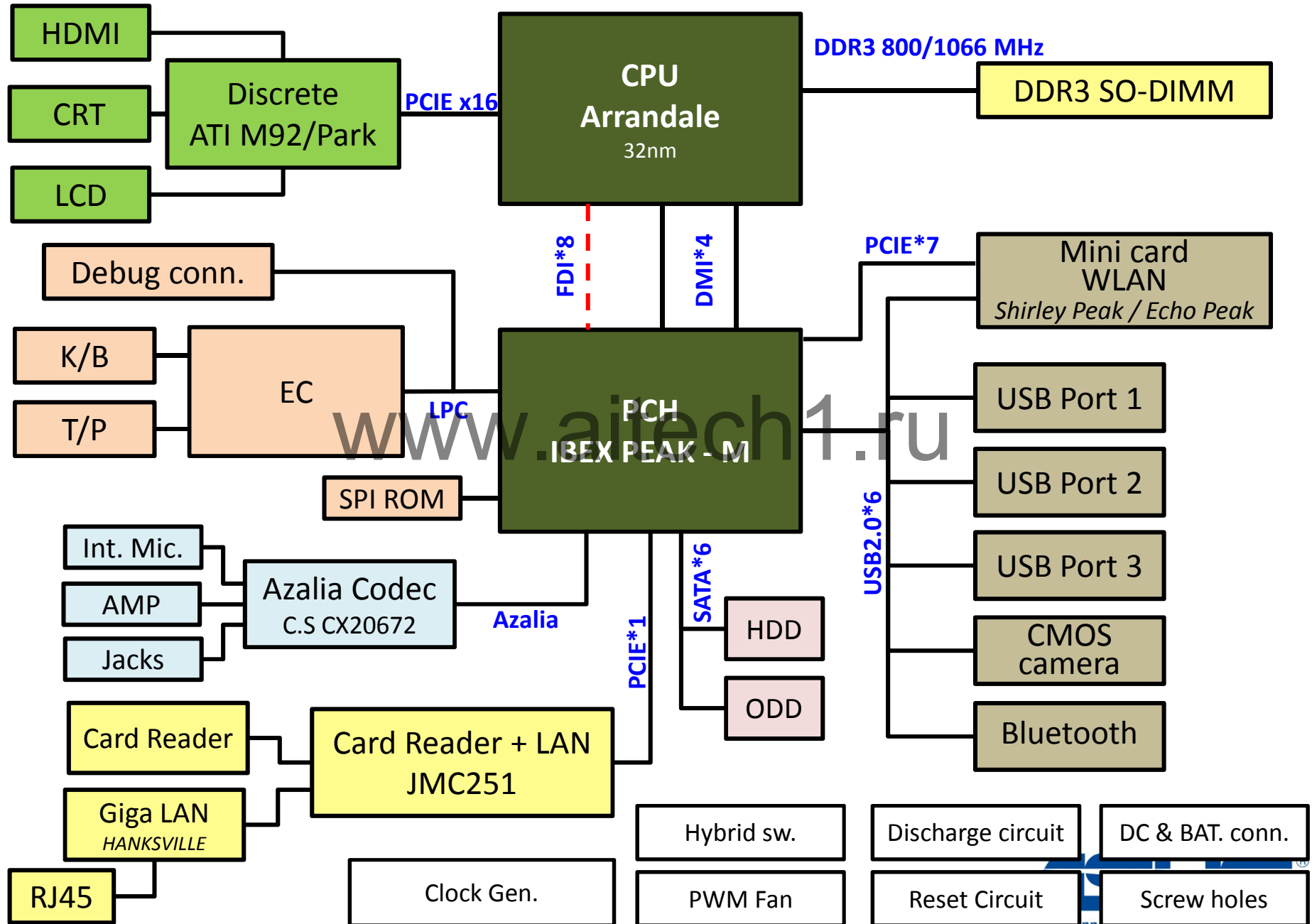


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Calpella Platform – K52JT Architecture



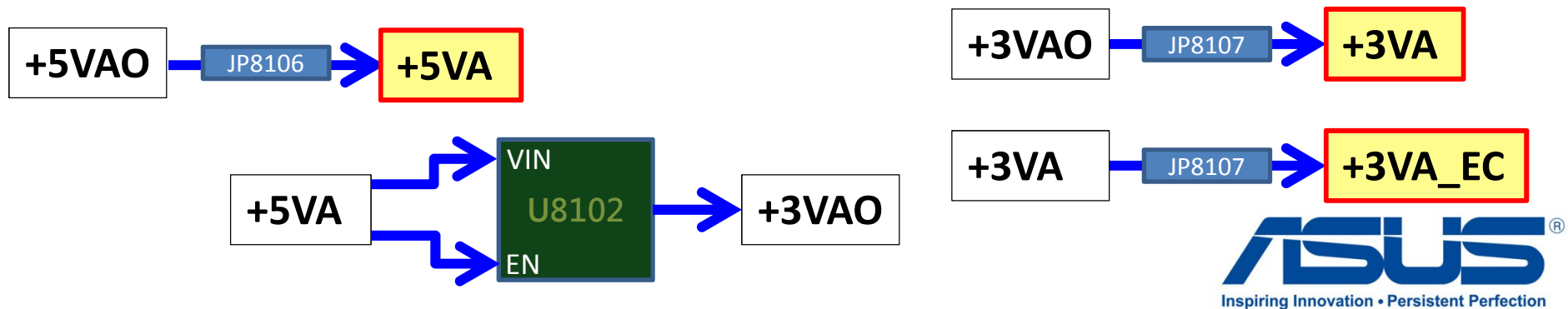
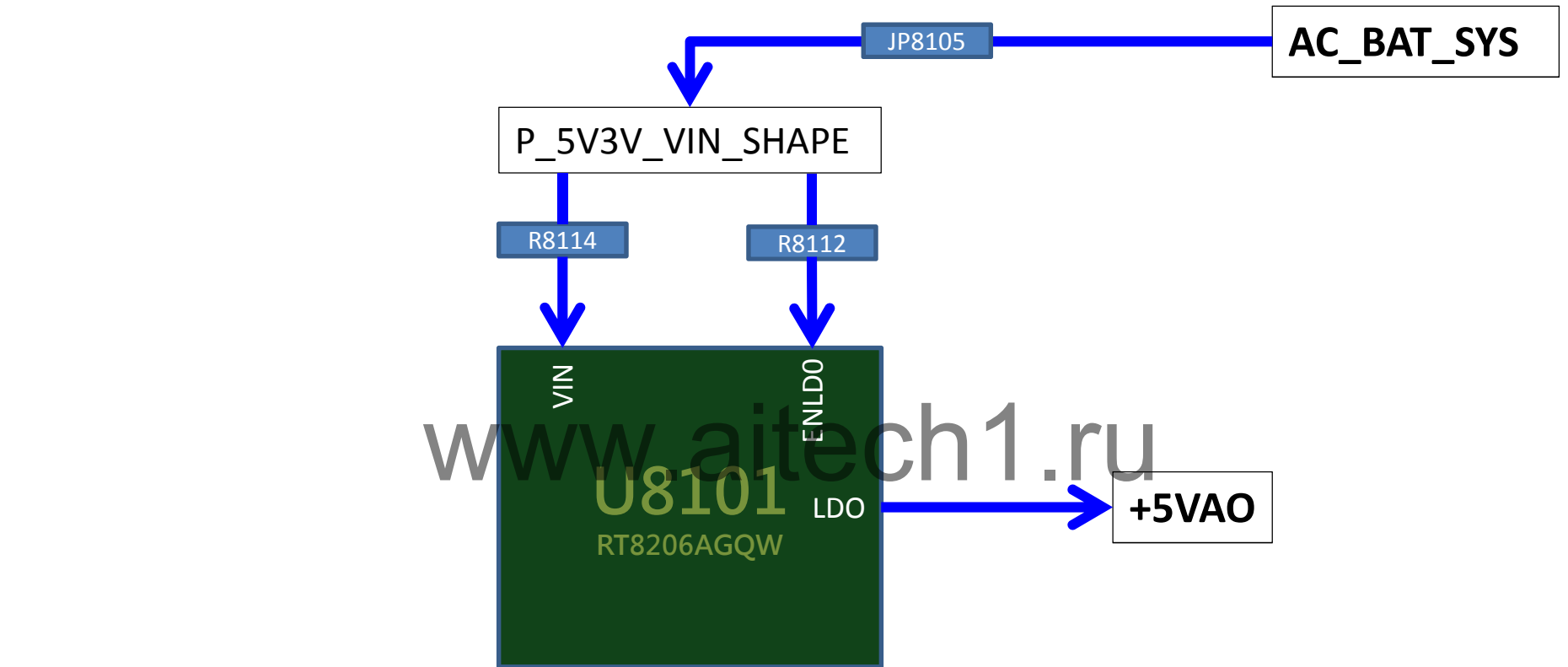
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No power

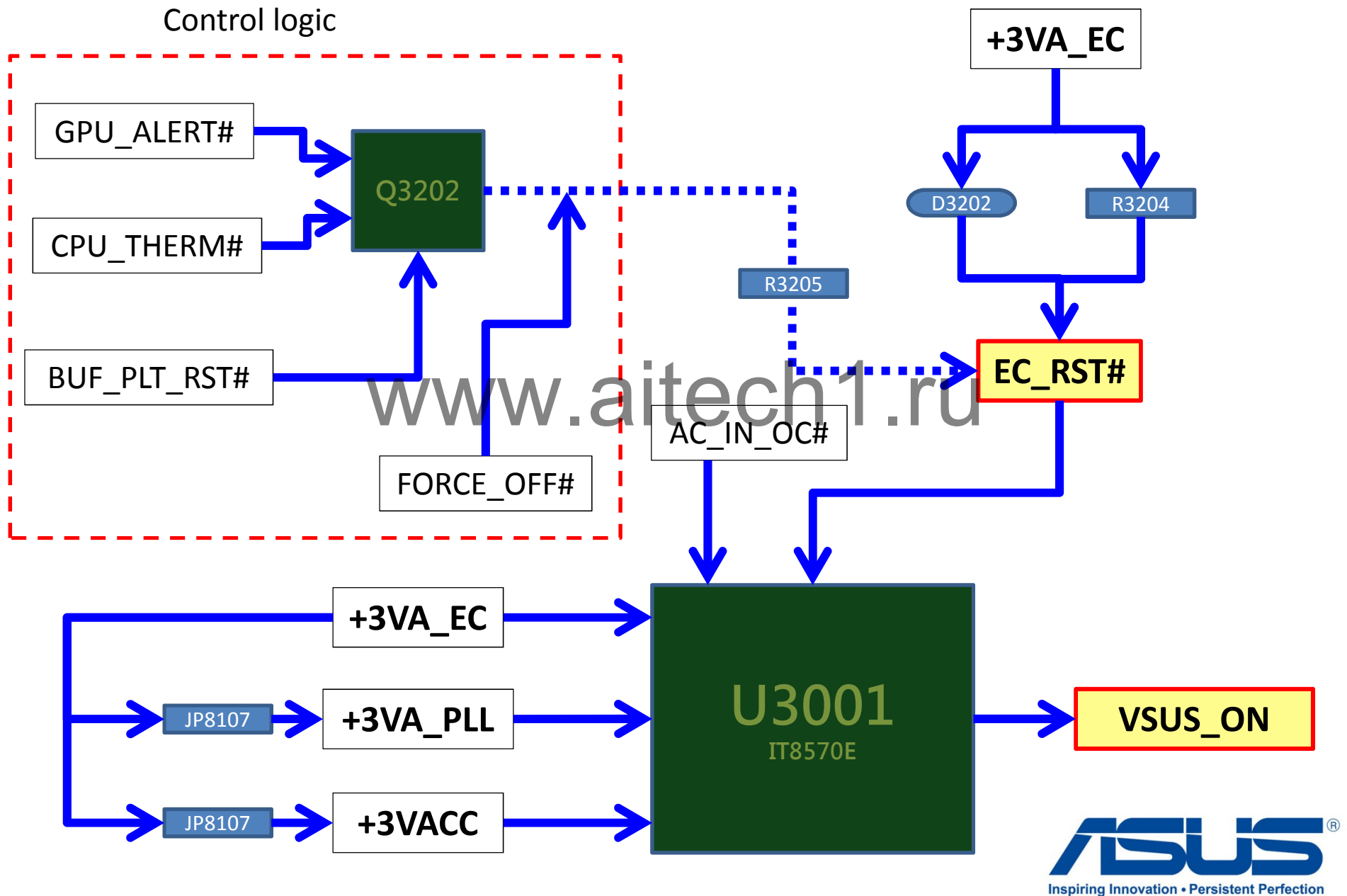
- Power on sequence analysis
- www.aitech1.ru AC IN Mode

➤ Power on sequence analysis *+3VA, +5VA, +3VA_EC*



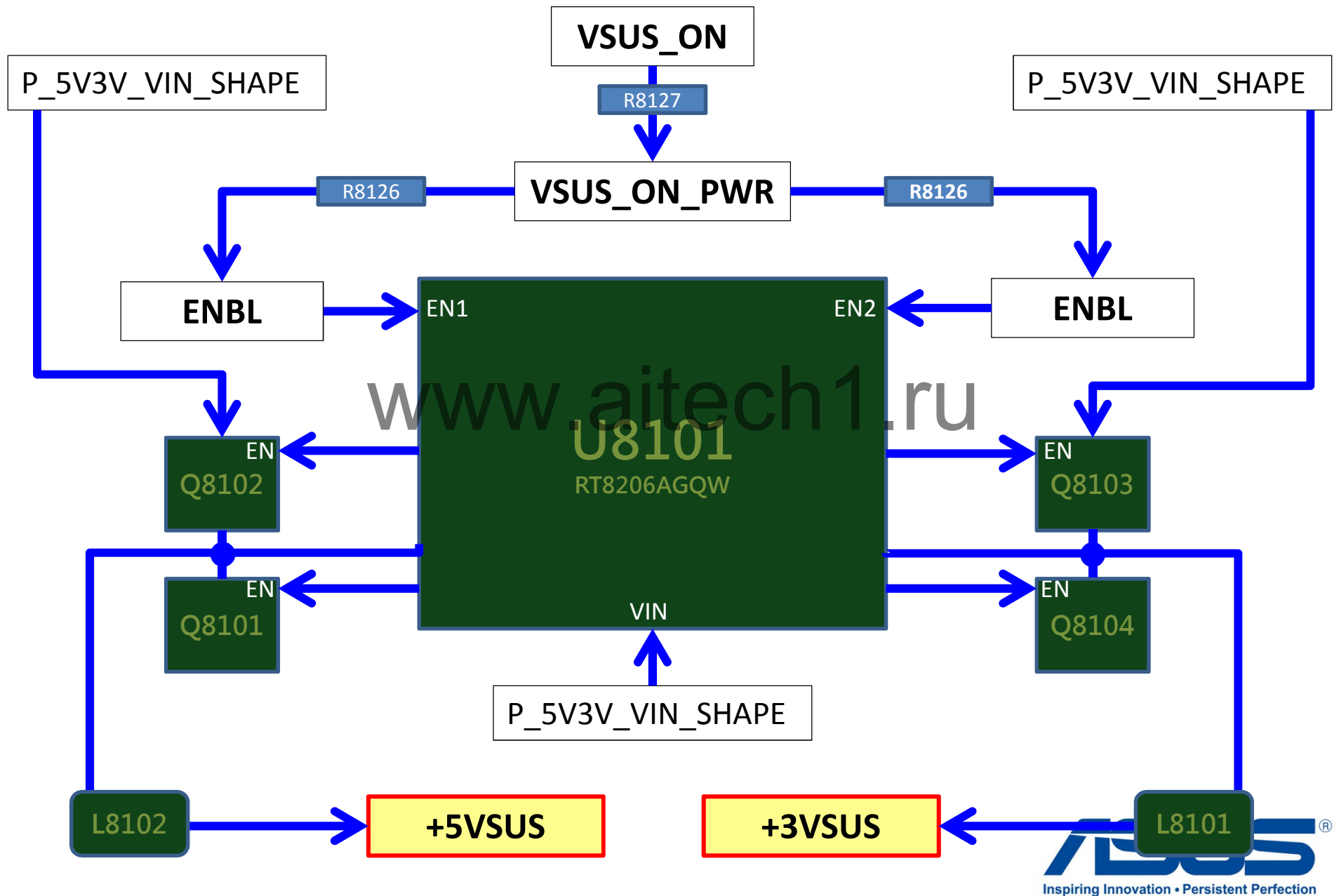
➤ Power on sequence analysis

EC_RST#, VSUS_ON



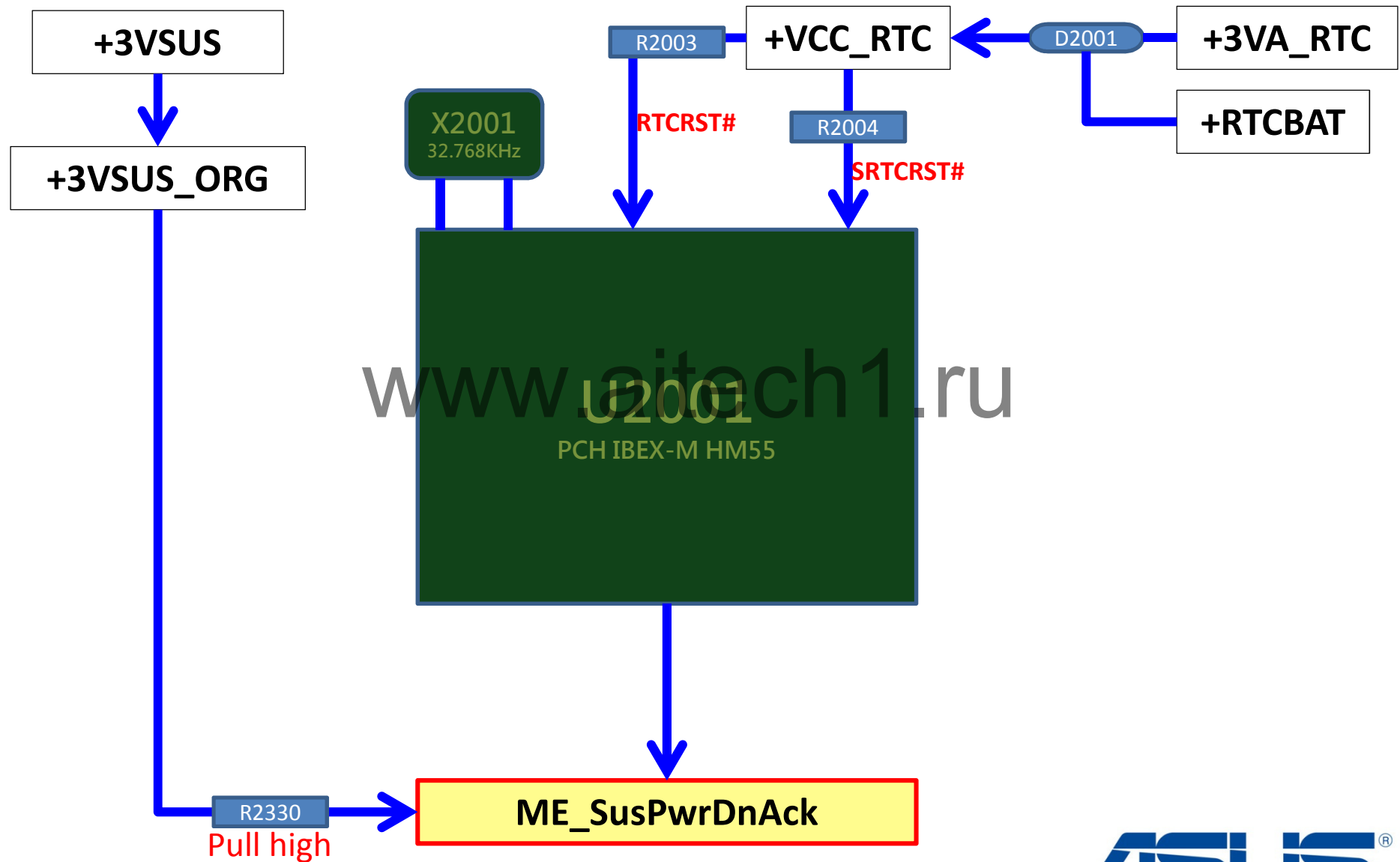
➤ Power on sequence analysis

+3VSUS, +5VSUS



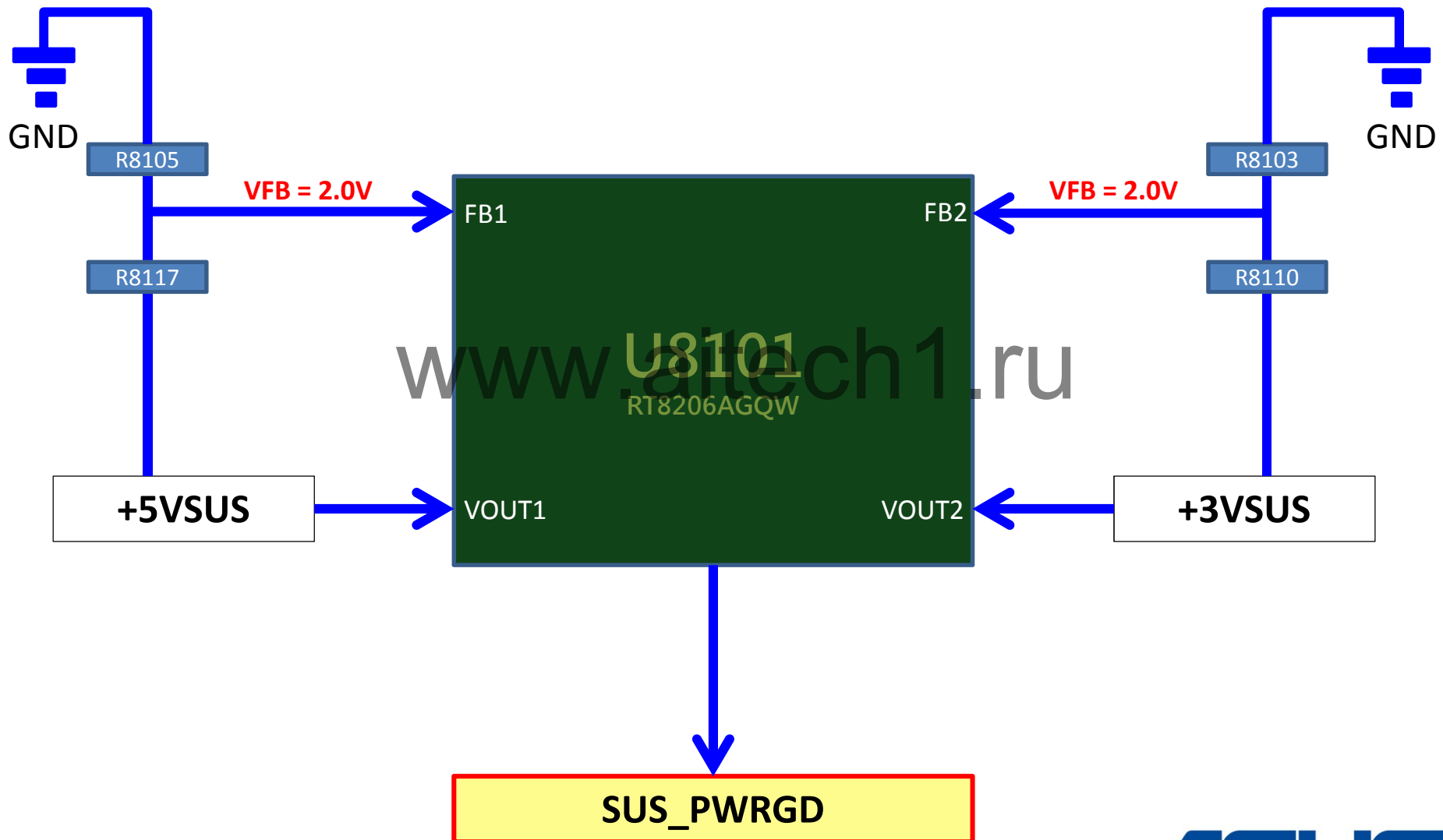
➤ Power on sequence analysis

ME_SusPwrDnAck



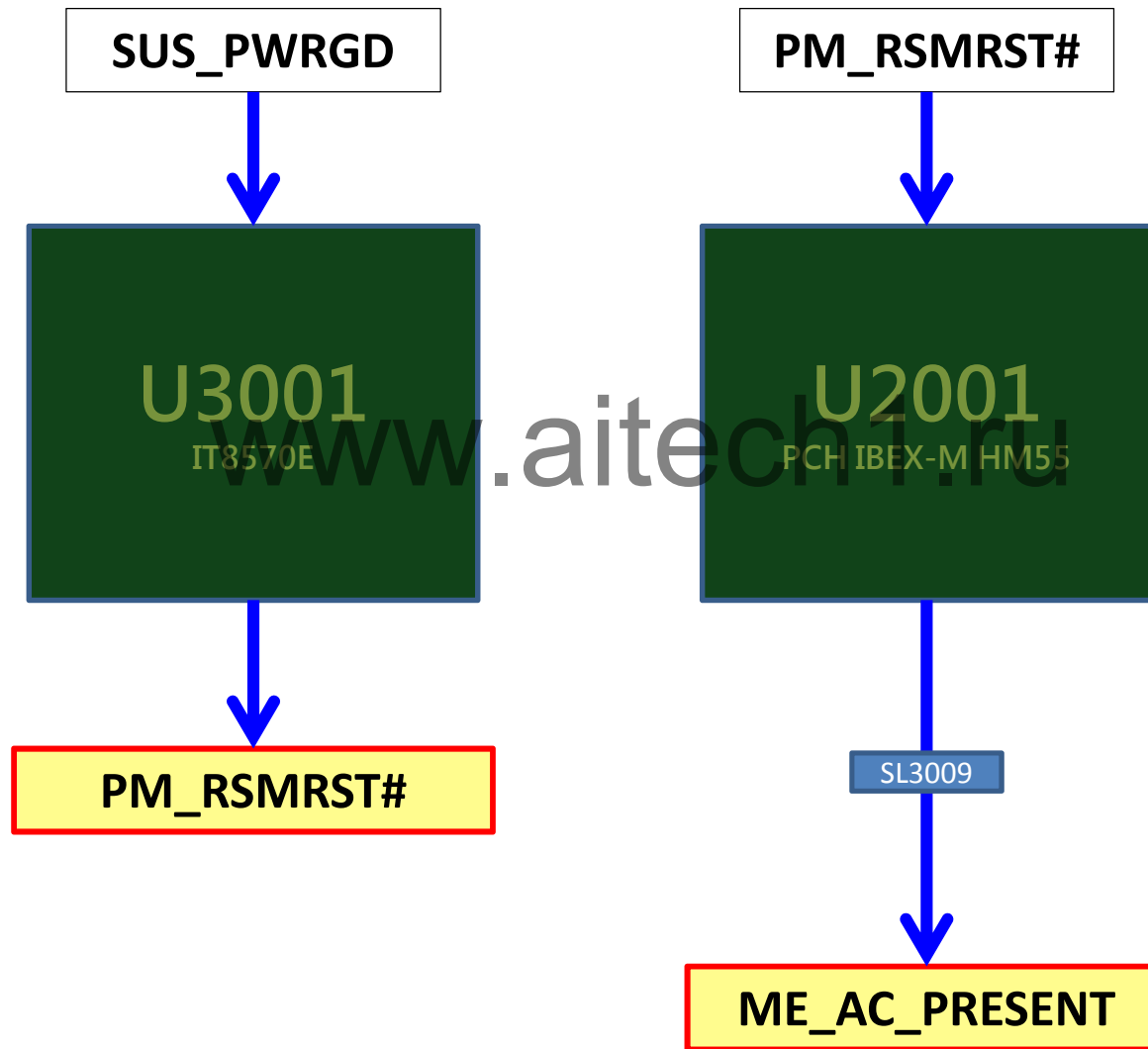
➤ Power on sequence analysis

SUS_PWRGD



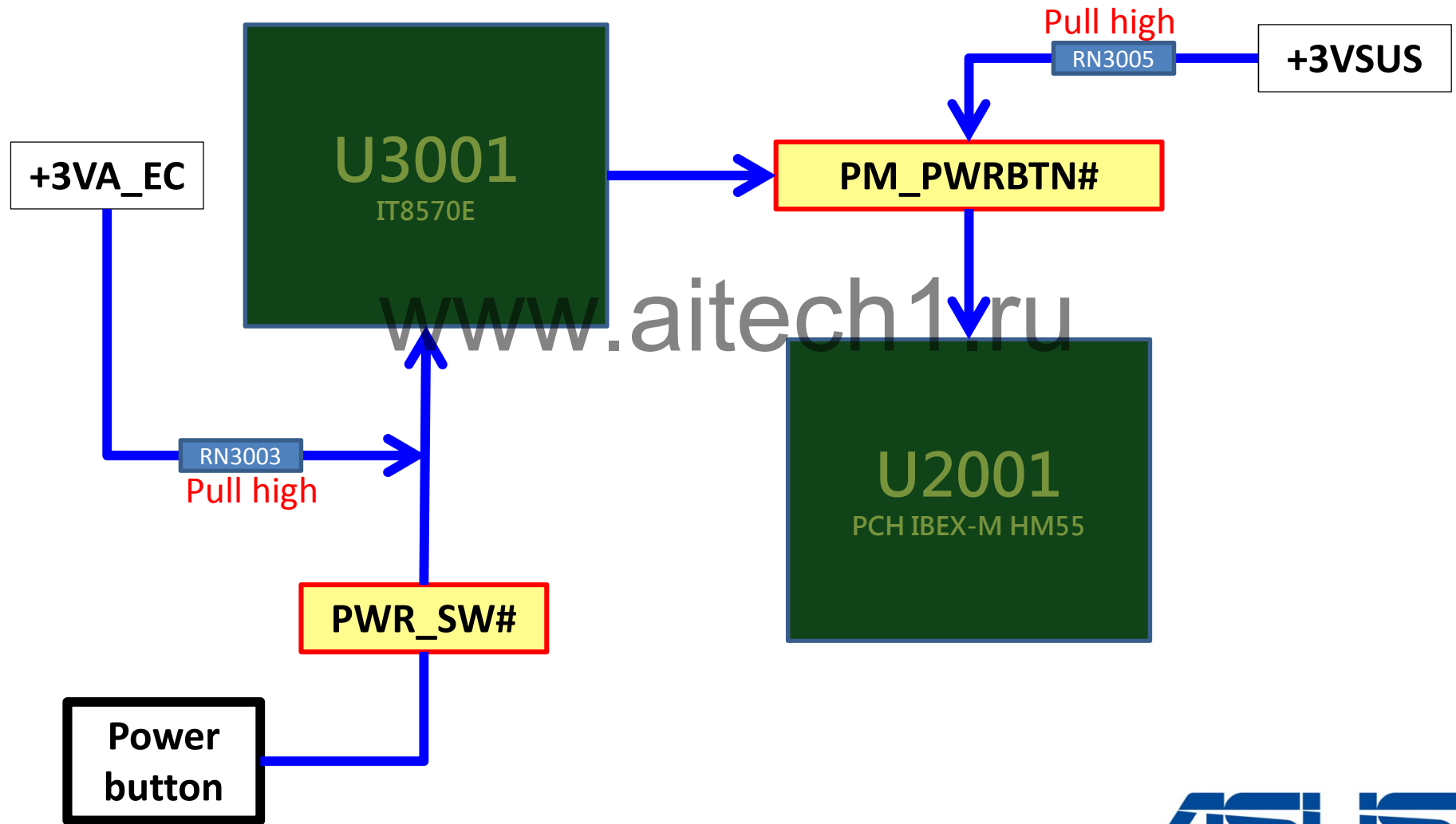
➤ Power on sequence analysis

PM_RSMRST#, ME_AC_PRESENT



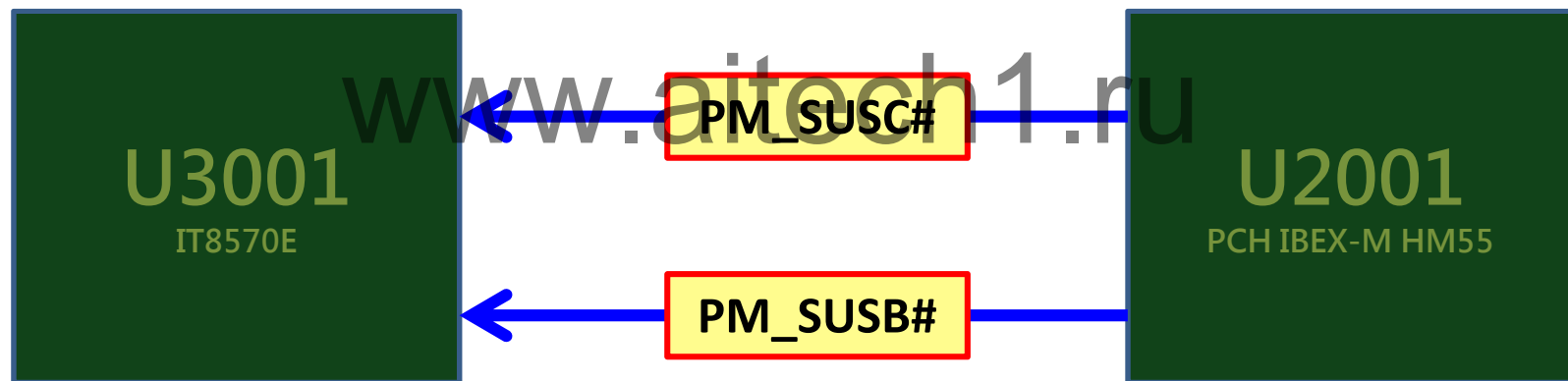
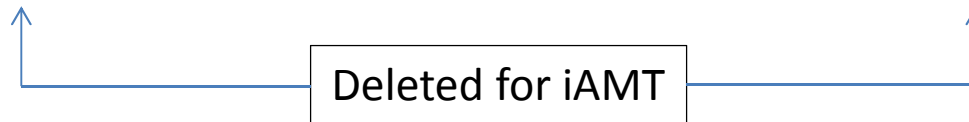
➤ Power on sequence analysis

PWR_SW#, PM_PWRBTN#



➤ Power on sequence analysis

~~ME_PM_SLP_M#~~, **PM_SUSC#**, ~~ME_PM_SLP_LAN#~~, **PM_SUSB#**

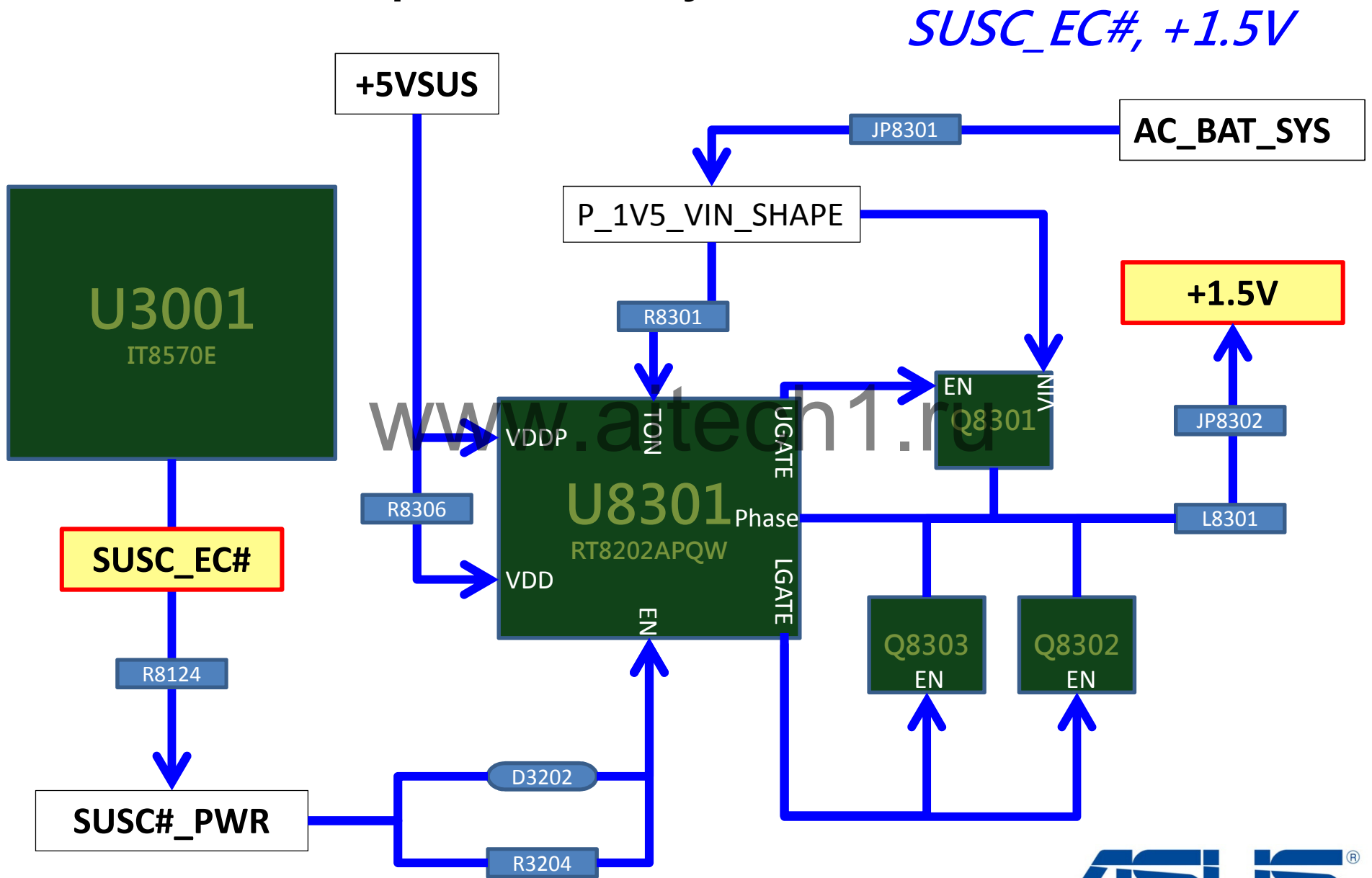


➤ Power on sequence analysis

~~+1.1VM, ME_SLP_M_EC#, +1.1VM, +3VM~~

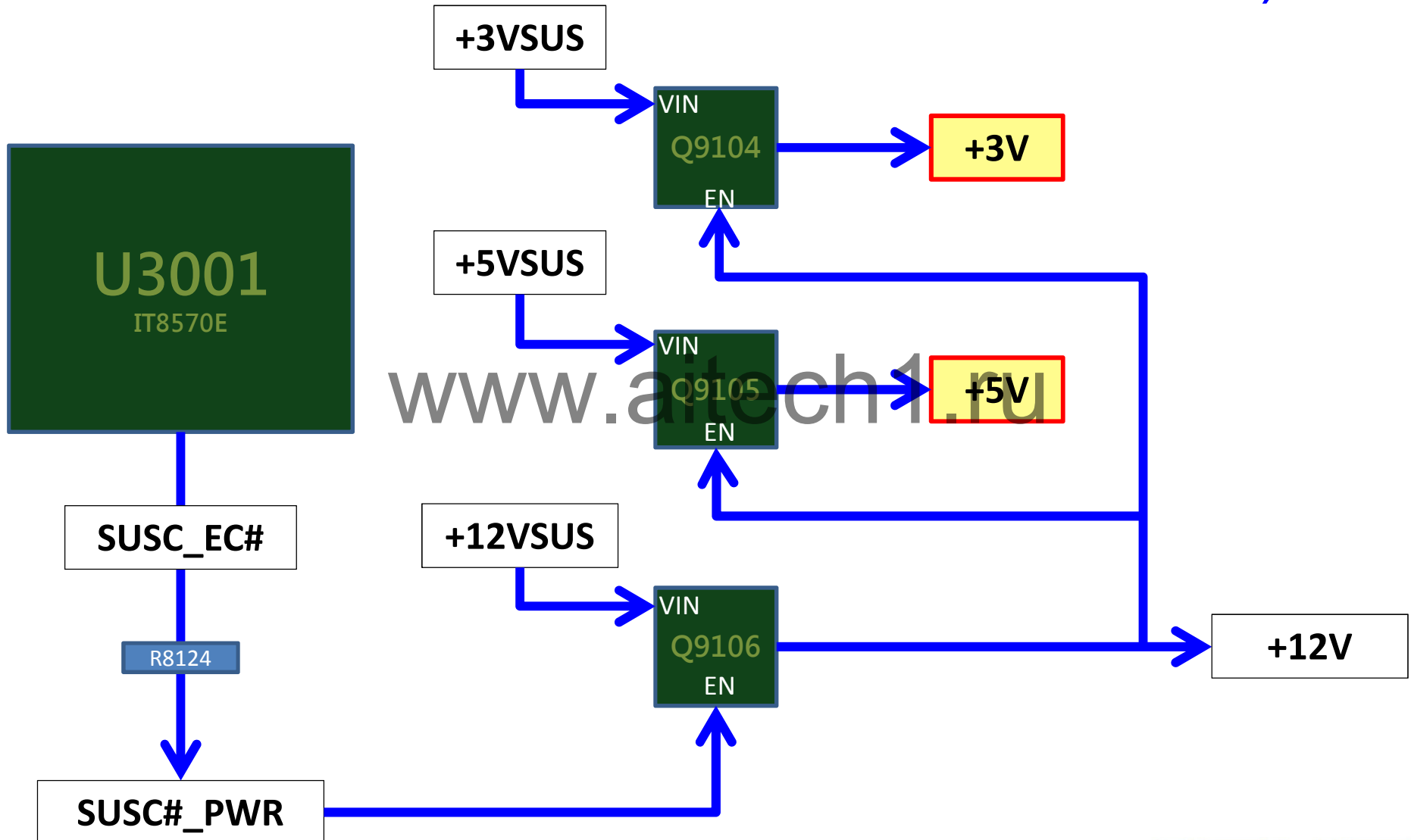
Deleted at all
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➤ Power on sequence analysis



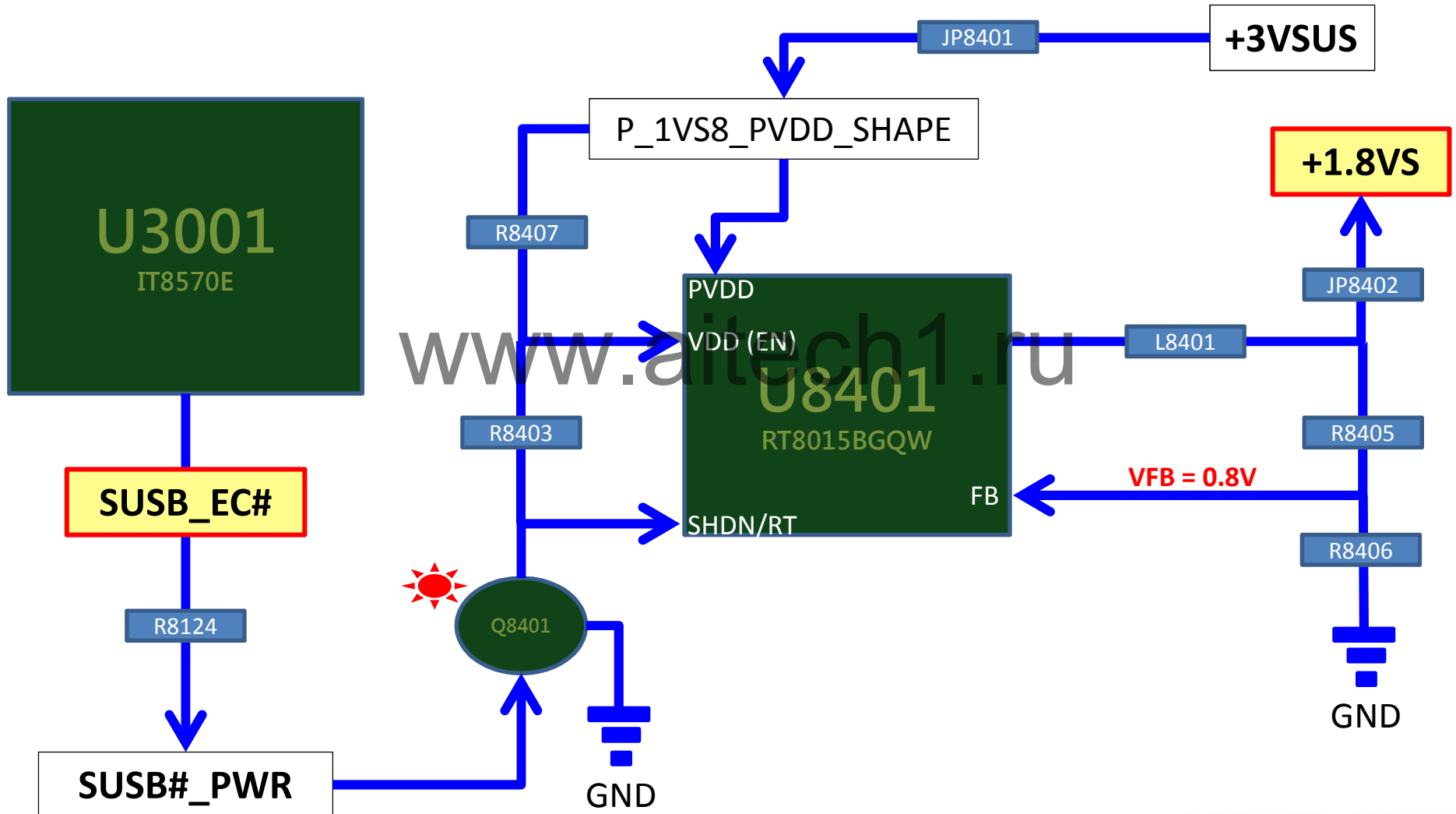
➤ Power on sequence analysis

$+3V, +5V$



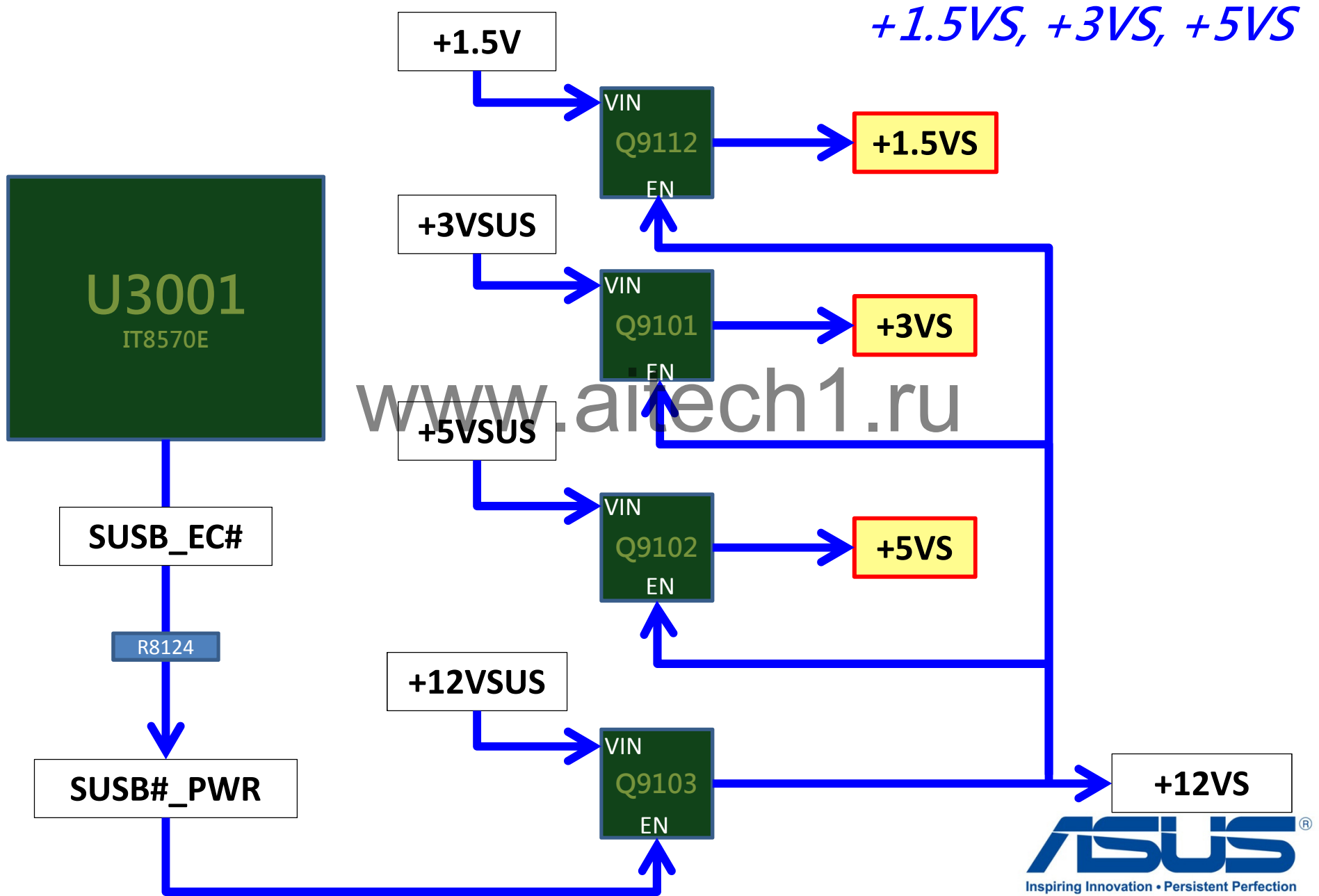
➤ Power on sequence analysis

SUSB_EC#, +1.8VS



 Q8401: A transistor to be the inverter.

➤ Power on sequence analysis



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No display with power is on

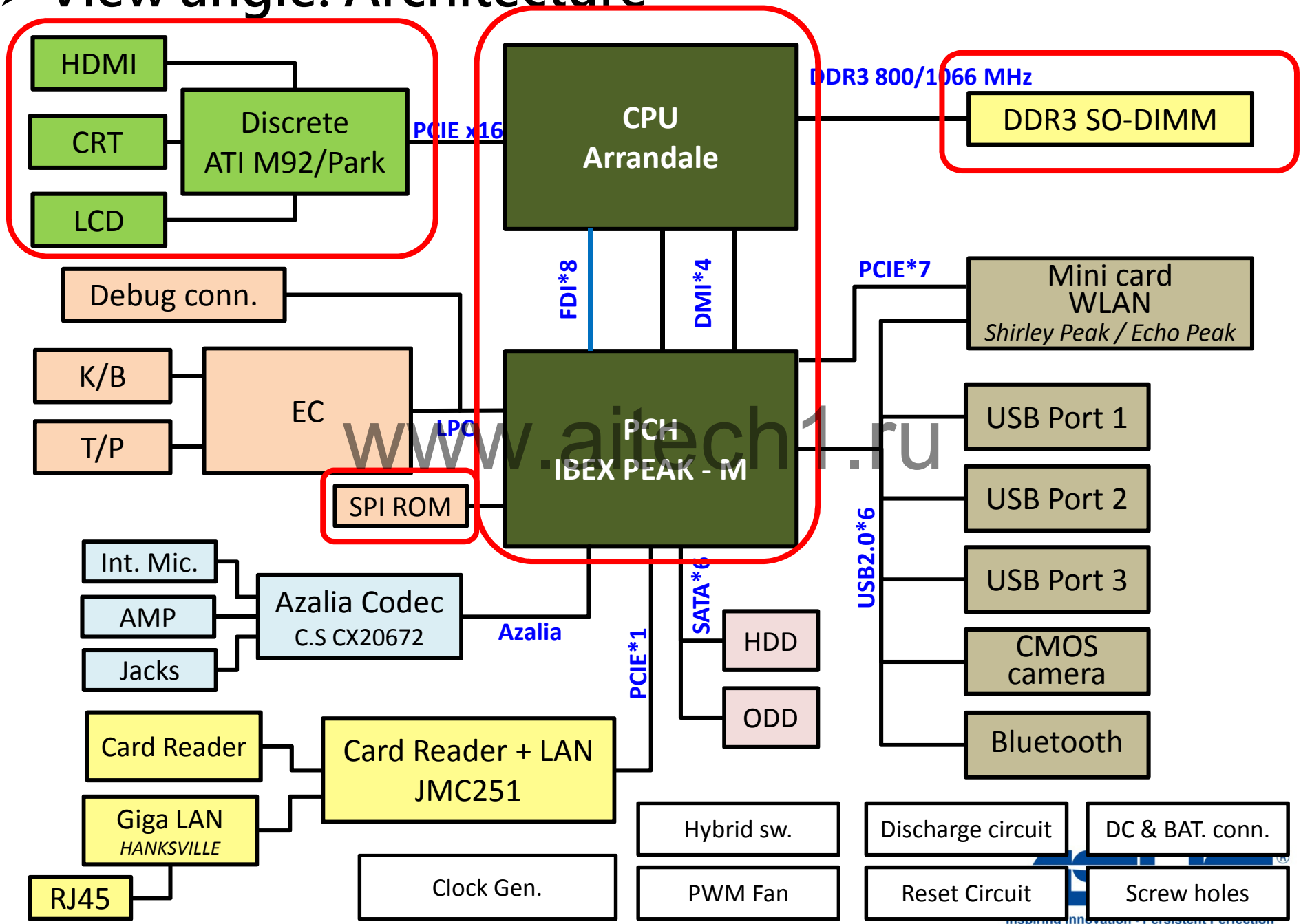
- View angle : Architecture
- Connection problems between GPU and display devices
- Connection problems between CPU and GPU
- No display due to BIOS problems
- Connection problems between PCH and CPU
- Connection problems between CPU and RAM(s)

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➤ View angle: Architecture



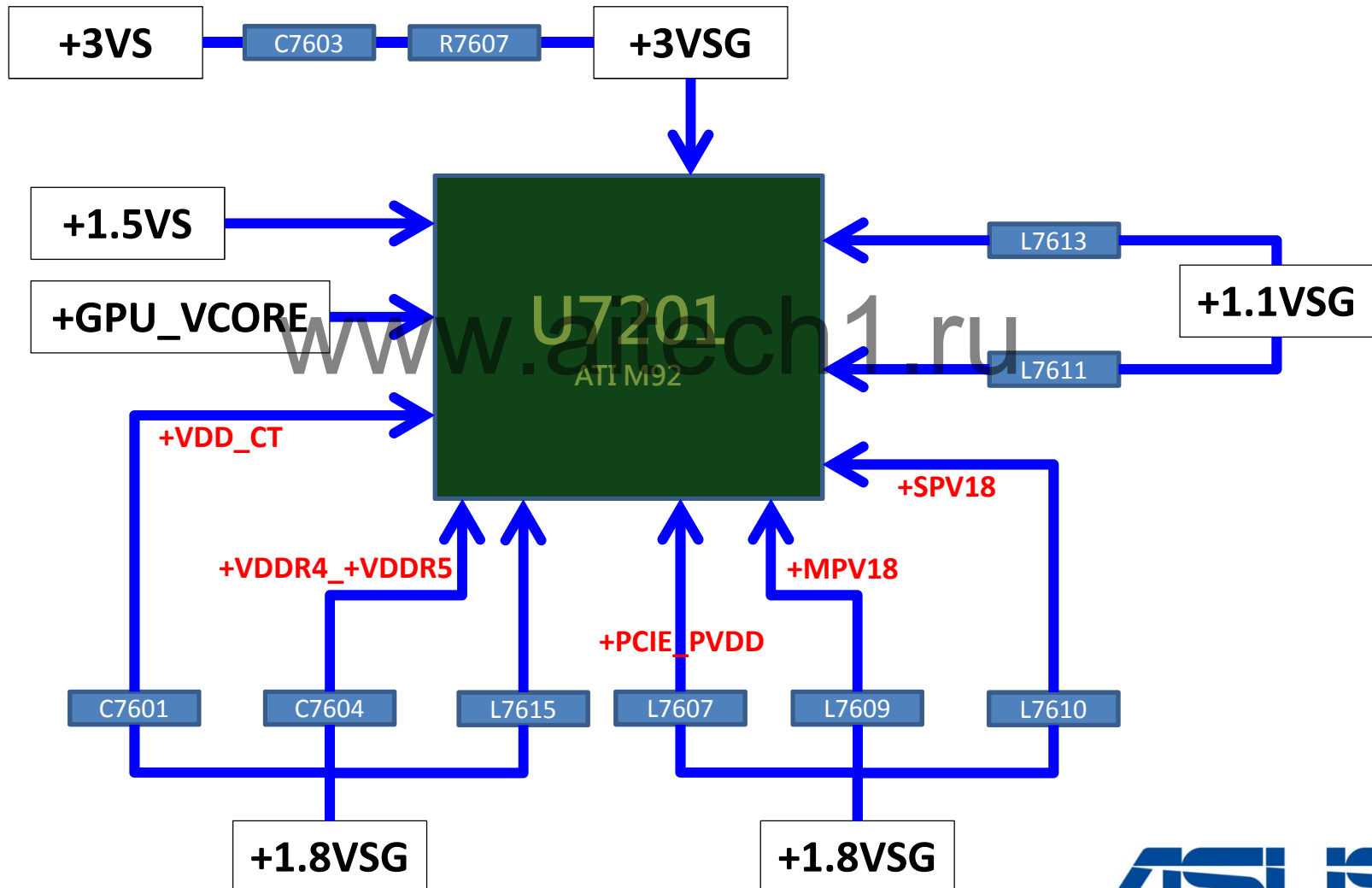
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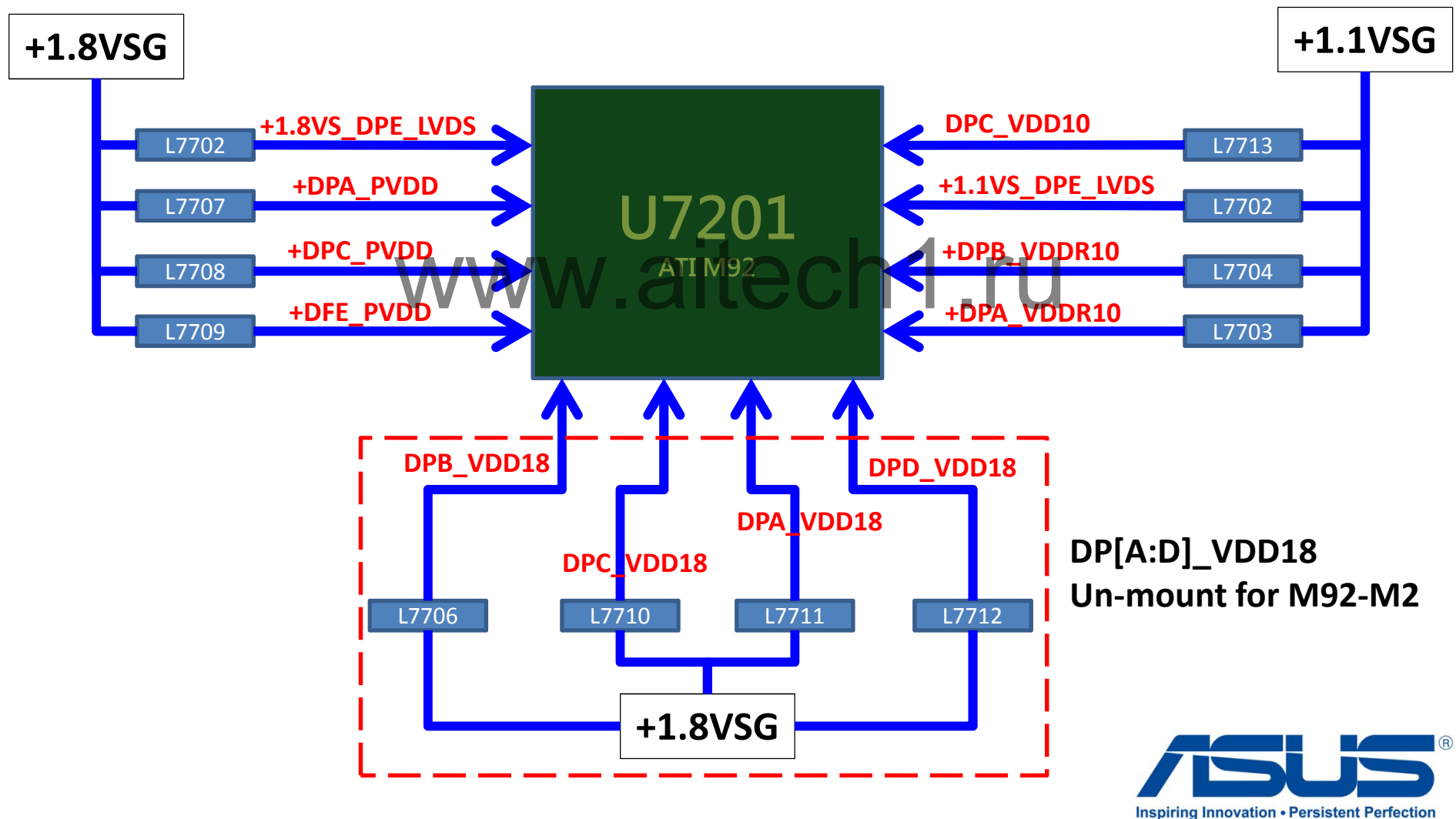
➤ Connection problems between GPU and display devices

Critical Power sources to ATI M92 GPU chipset(1)



➤ Connection problems between GPU and display devices

Critical Power sources to ATI M92 GPU chipset(2)



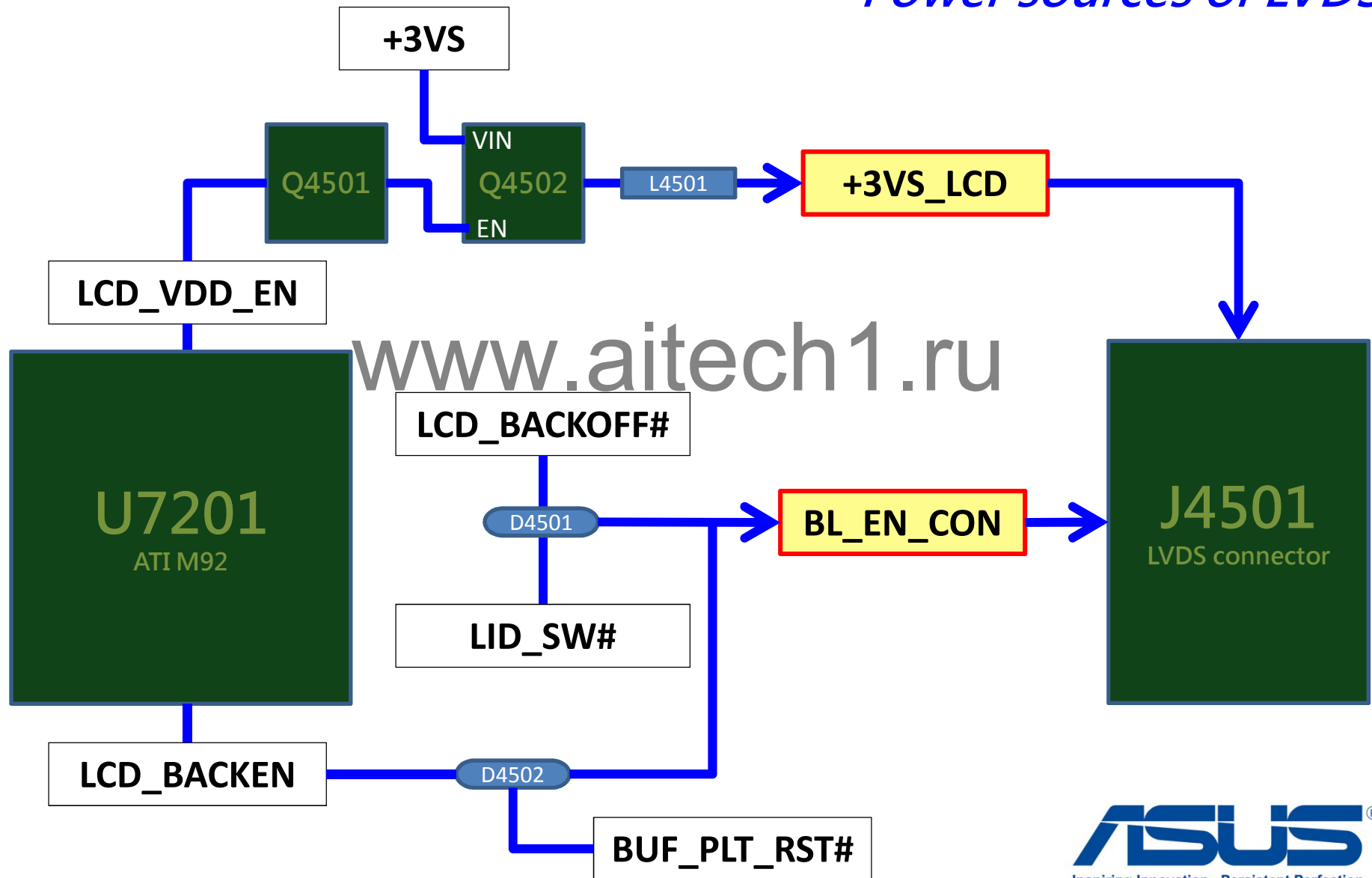
➤ Connection problems between GPU and display devices

Critical Clocks to ATI M92 GPU chipset



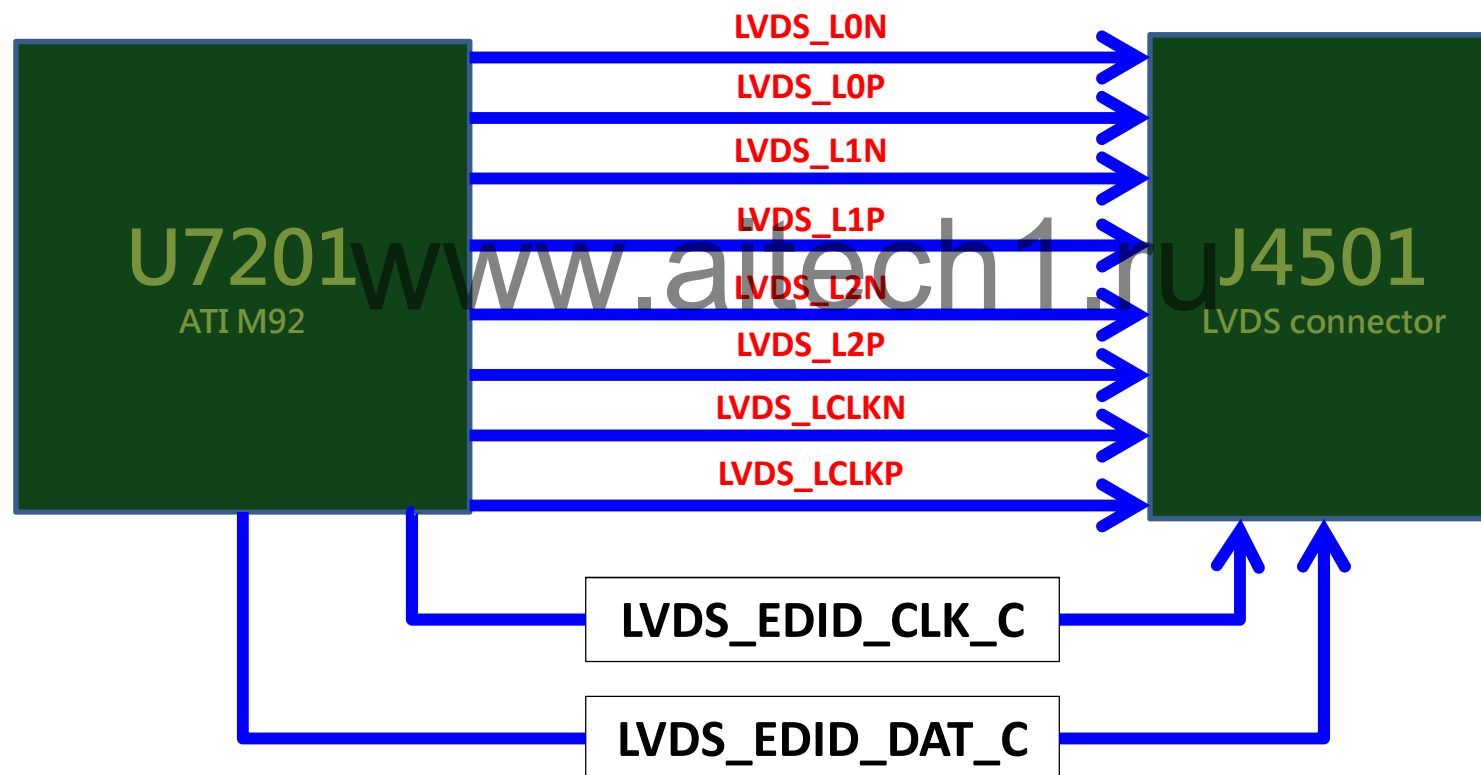
➤ Connection problems between GPU and display devices

Power sources of LVDS



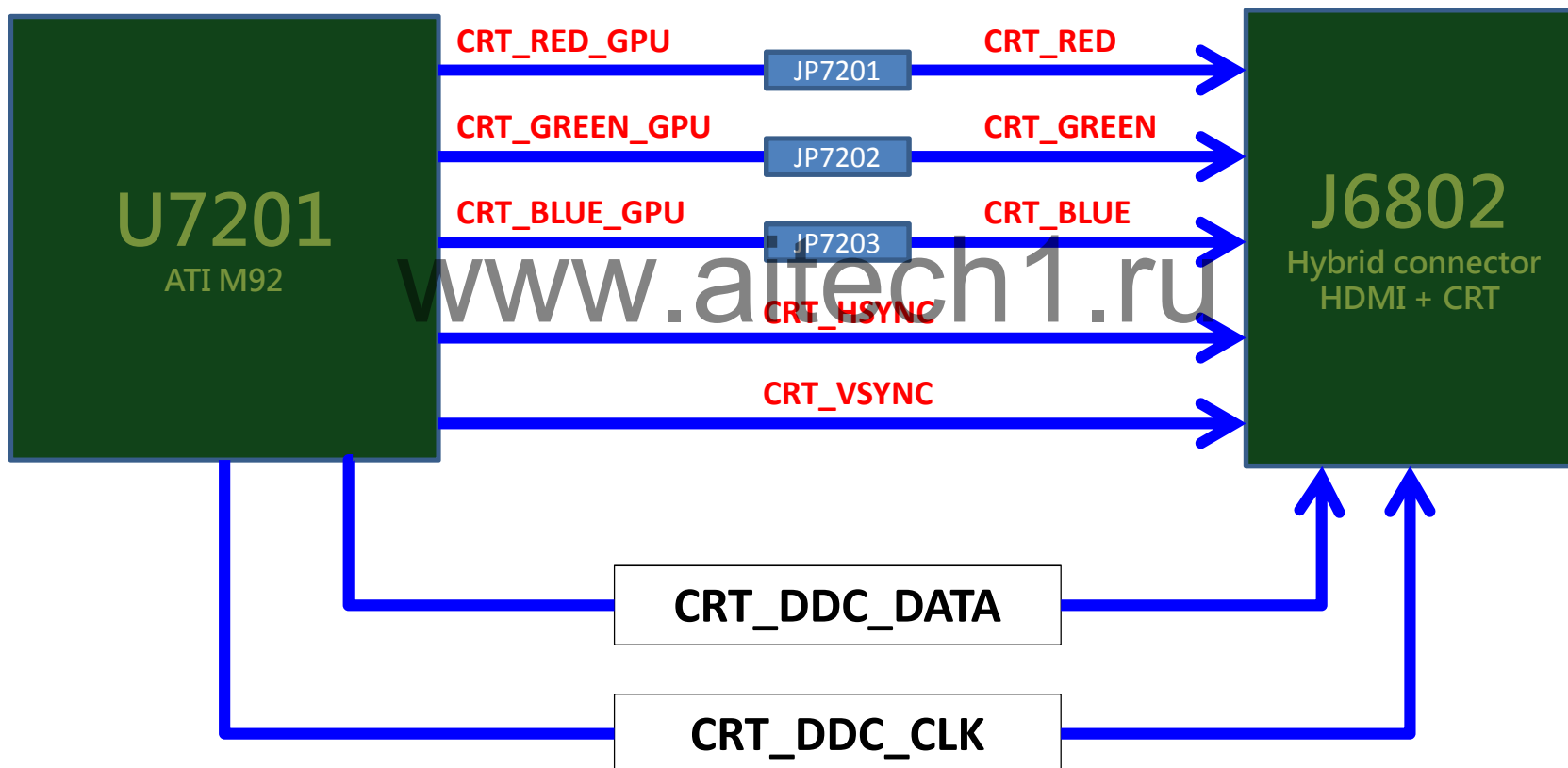
➤ Connection problems between GPU and display devices

Signals from GPU to LVDS



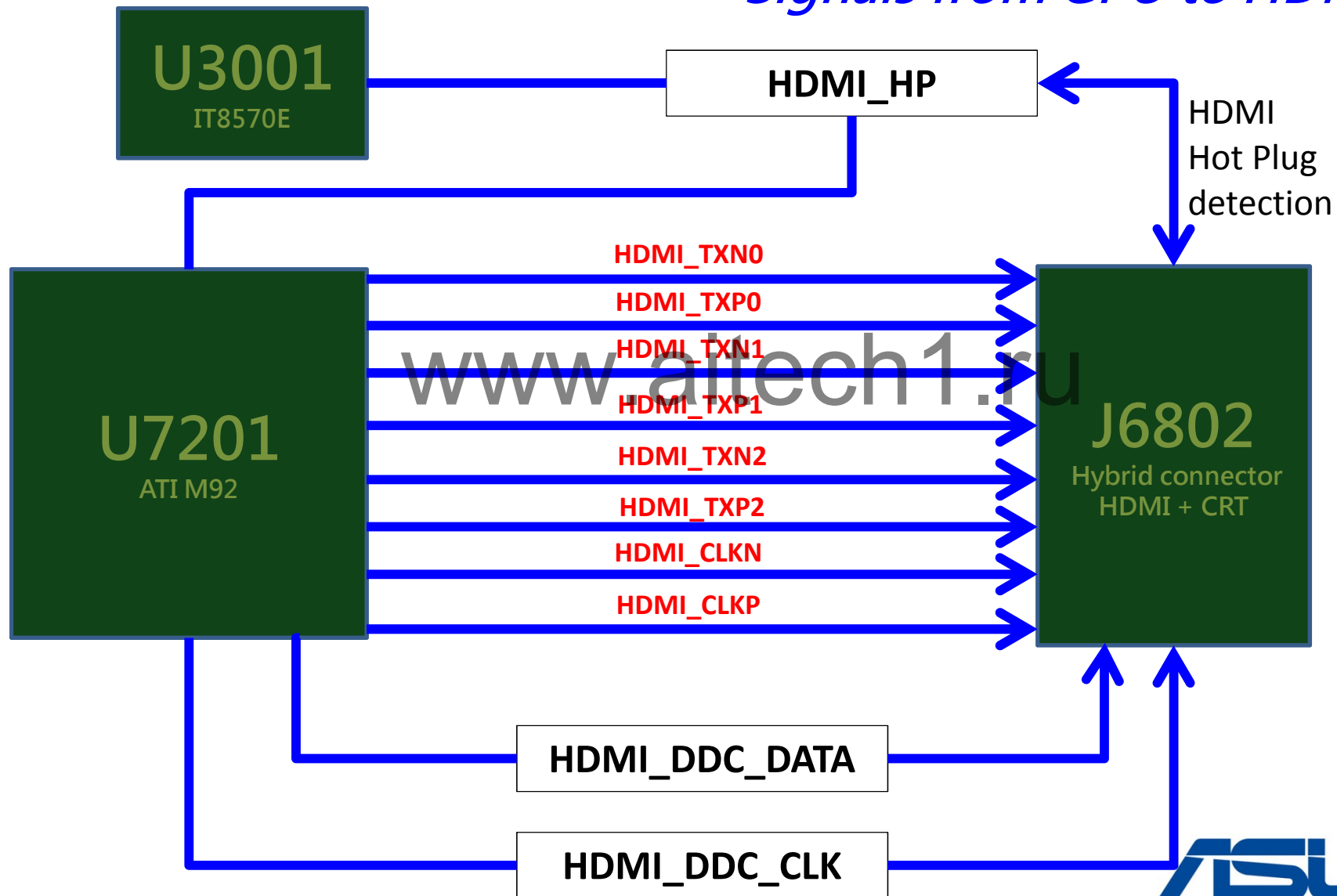
➤ Connection problems between GPU and display devices

Signals from GPU to CRT out



➤ Connection problems between GPU and display devices

Signals from GPU to HDMI out



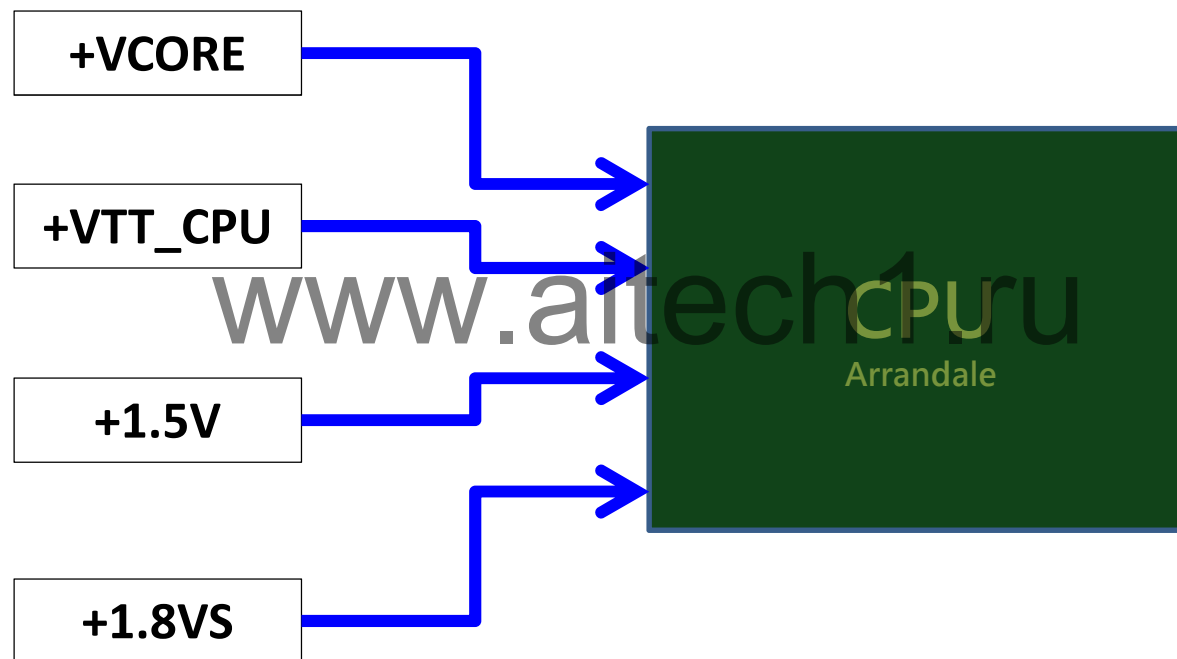
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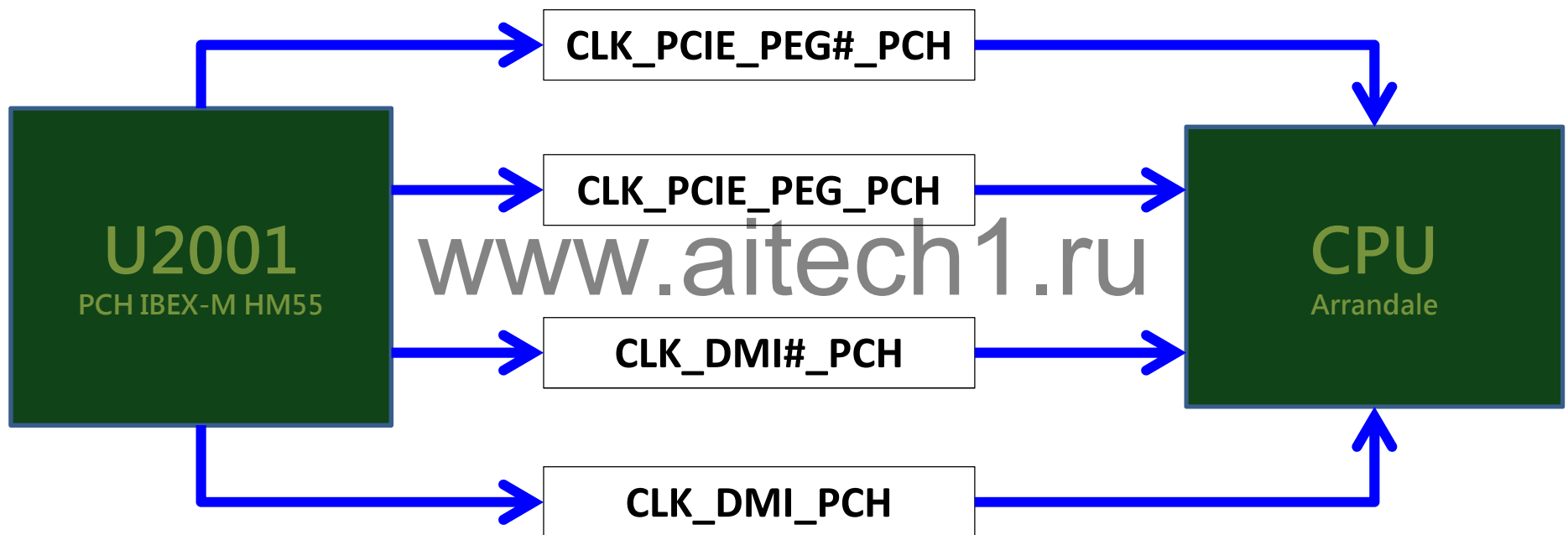
➤ Connection problems between CPU and GPU

Critical Power sources to CPU



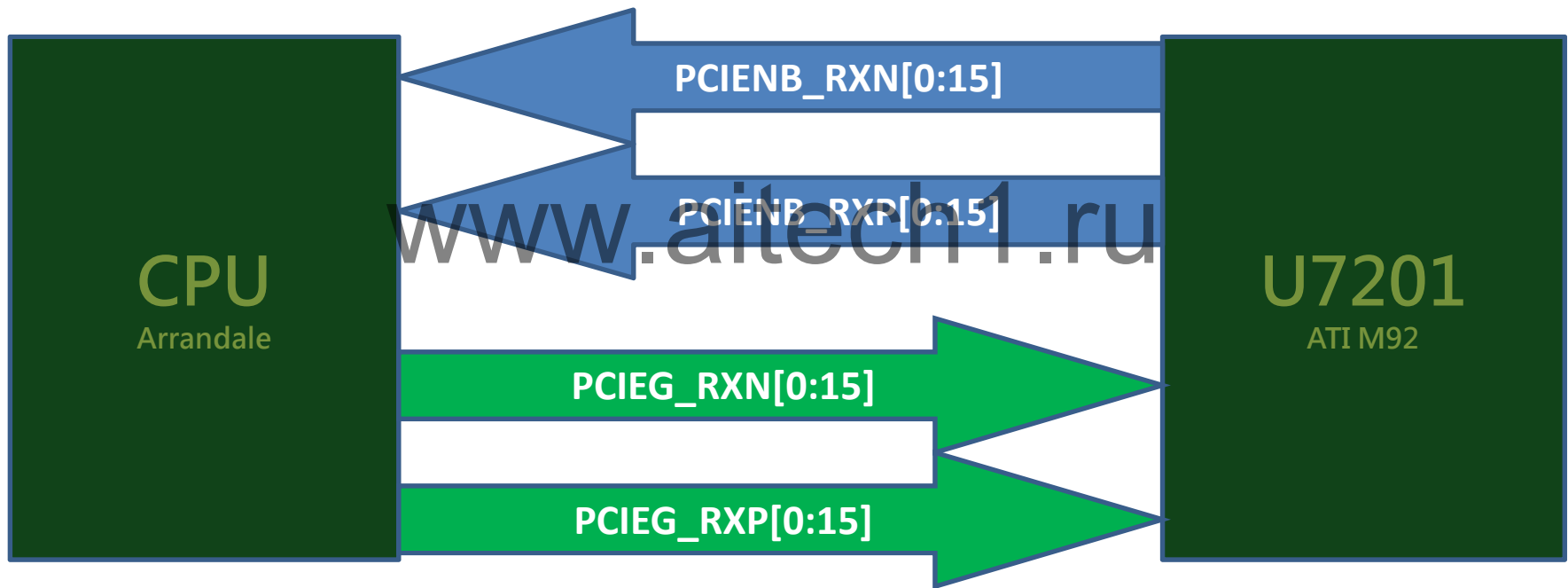
➤ Connection problems between CPU and GPU

Critical Clocks from PCH to CPU



➤ Connection problems between CPU and GPU

Data Transmission pins between CPU & GPU

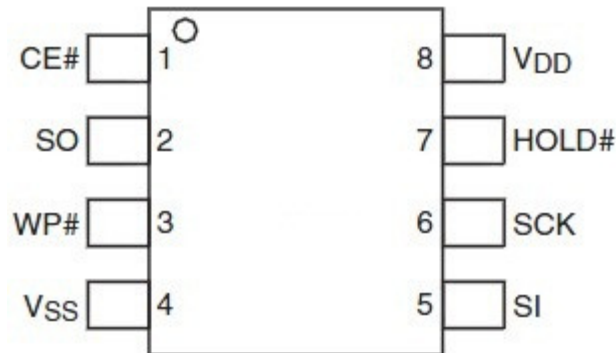


No display with power is on

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➤ No display due to BIOS problems

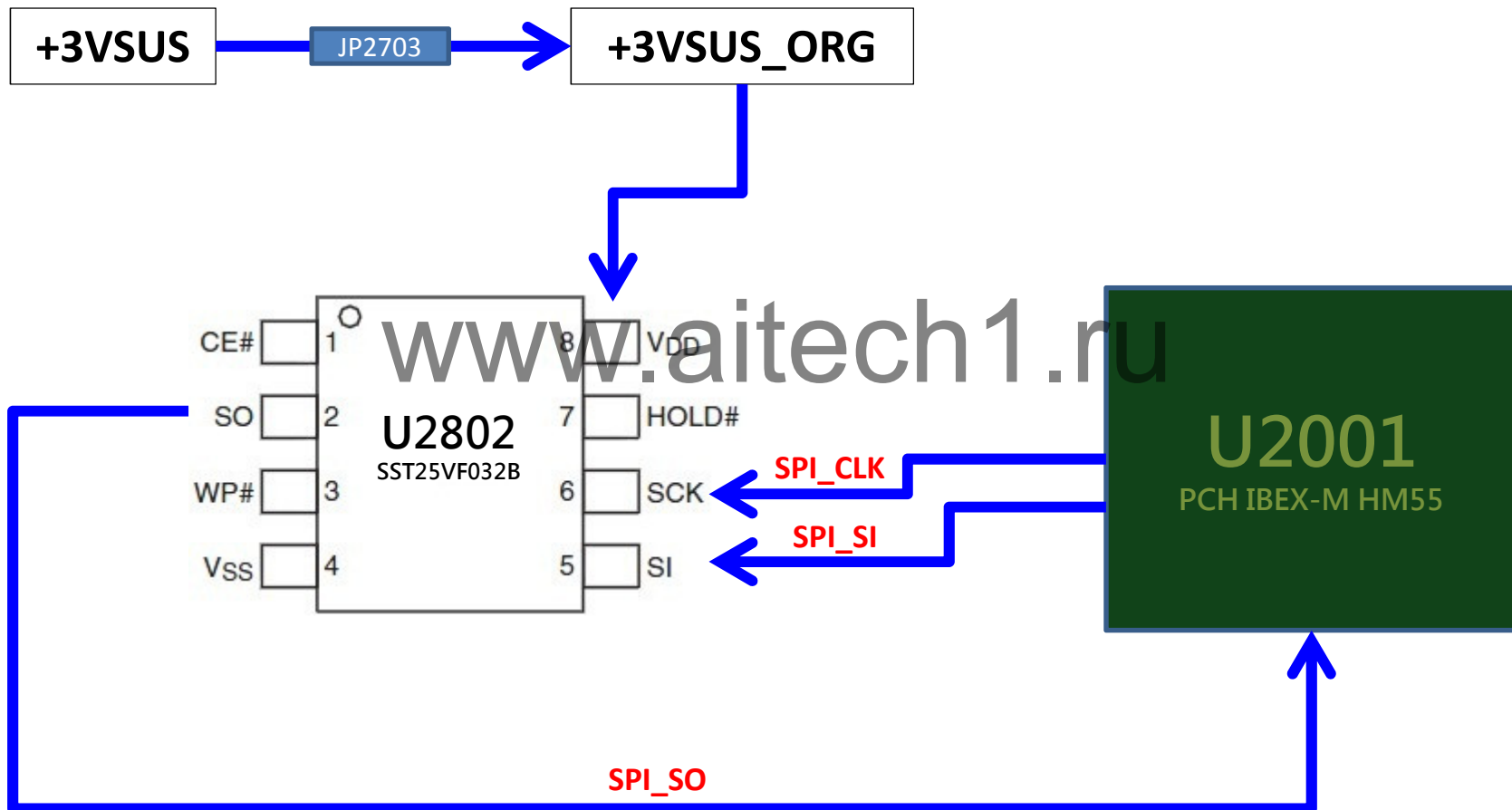
SST 25VF032B Pin Descriptions



Symbol	Pin Name	Functions
SCK	Serial Clock	To provide the timing of the serial interface. Commands, addresses, or input data are latched on the rising edge of the clock input, while output data is shifted out on the falling edge of the clock input.
SI	Serial Data Input	To transfer commands, addresses, or data serially into the device. Inputs are latched on the rising edge of the serial clock.
SO	Serial Data Output	To transfer data serially out of the device. Data is shifted out on the falling edge of the serial clock.
CE#	Chip Enable	The device is enabled by a high to low transition on CE#. CE# must remain low for the duration of any command sequence.
WP#	Write Protect	The Write Protect (WP#) pin is used to enable/disable BPL bit in the status register.
HOLD#	Hold	To temporarily stop serial communication with SPI flash memory without resetting the device.
V _{DD}	Power Supply	To provide power supply voltage: 2.7-3.6V
V _{SS}	Ground	

➤ No display due to BIOS problems

How BIOS works in K52JT



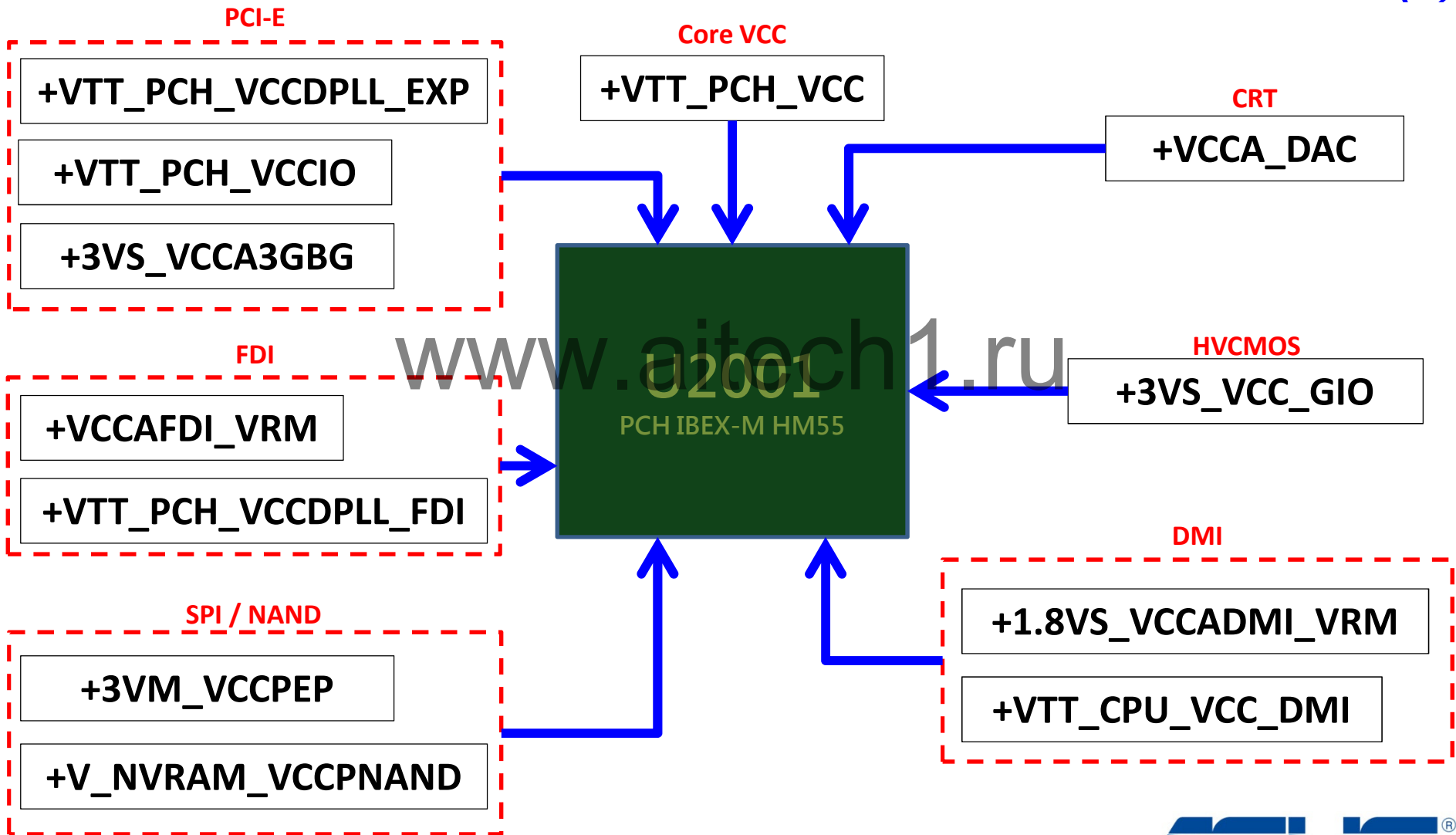
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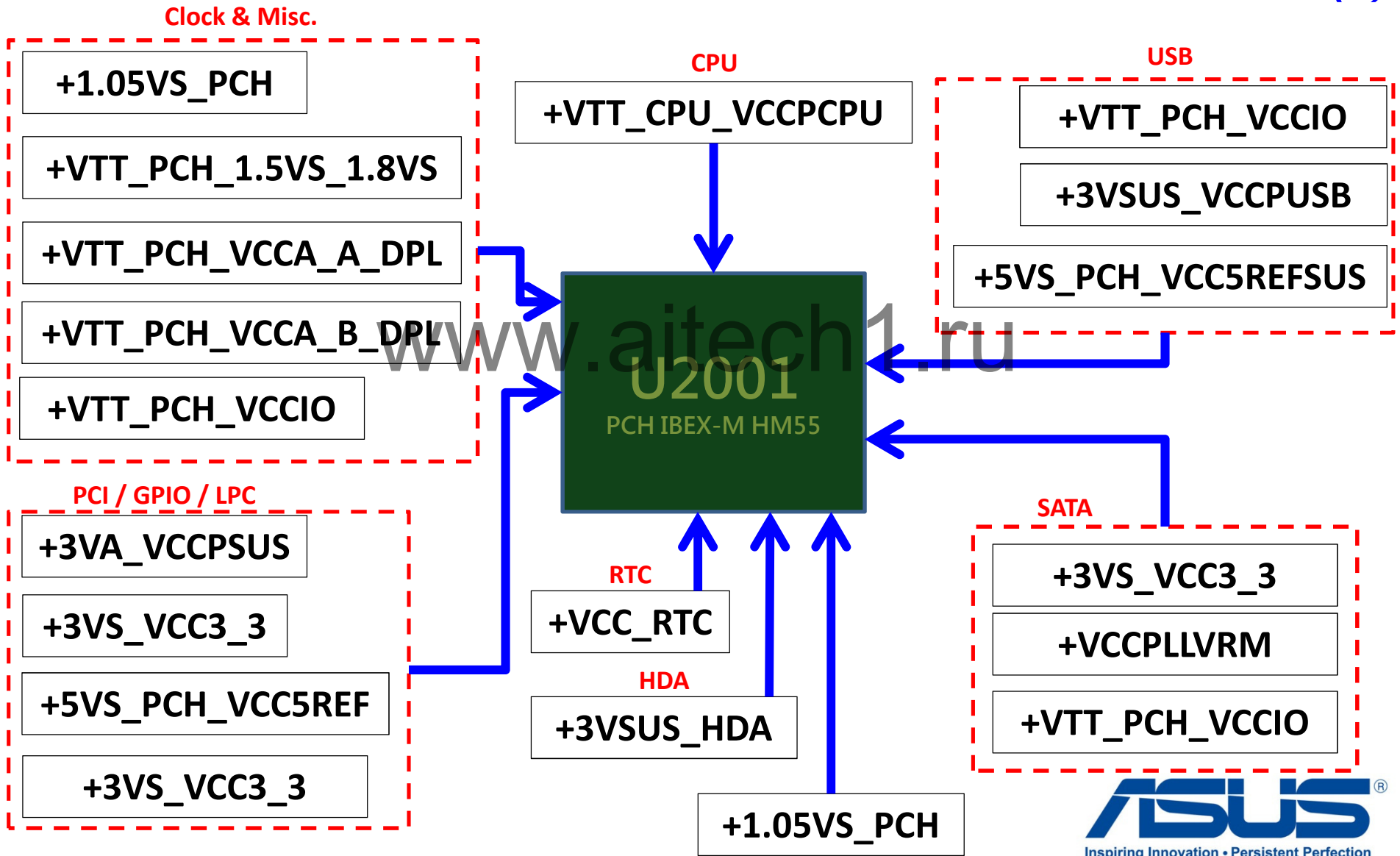
➤ Connection problems between PCH and CPU

Critical Power sources to PCH (1)



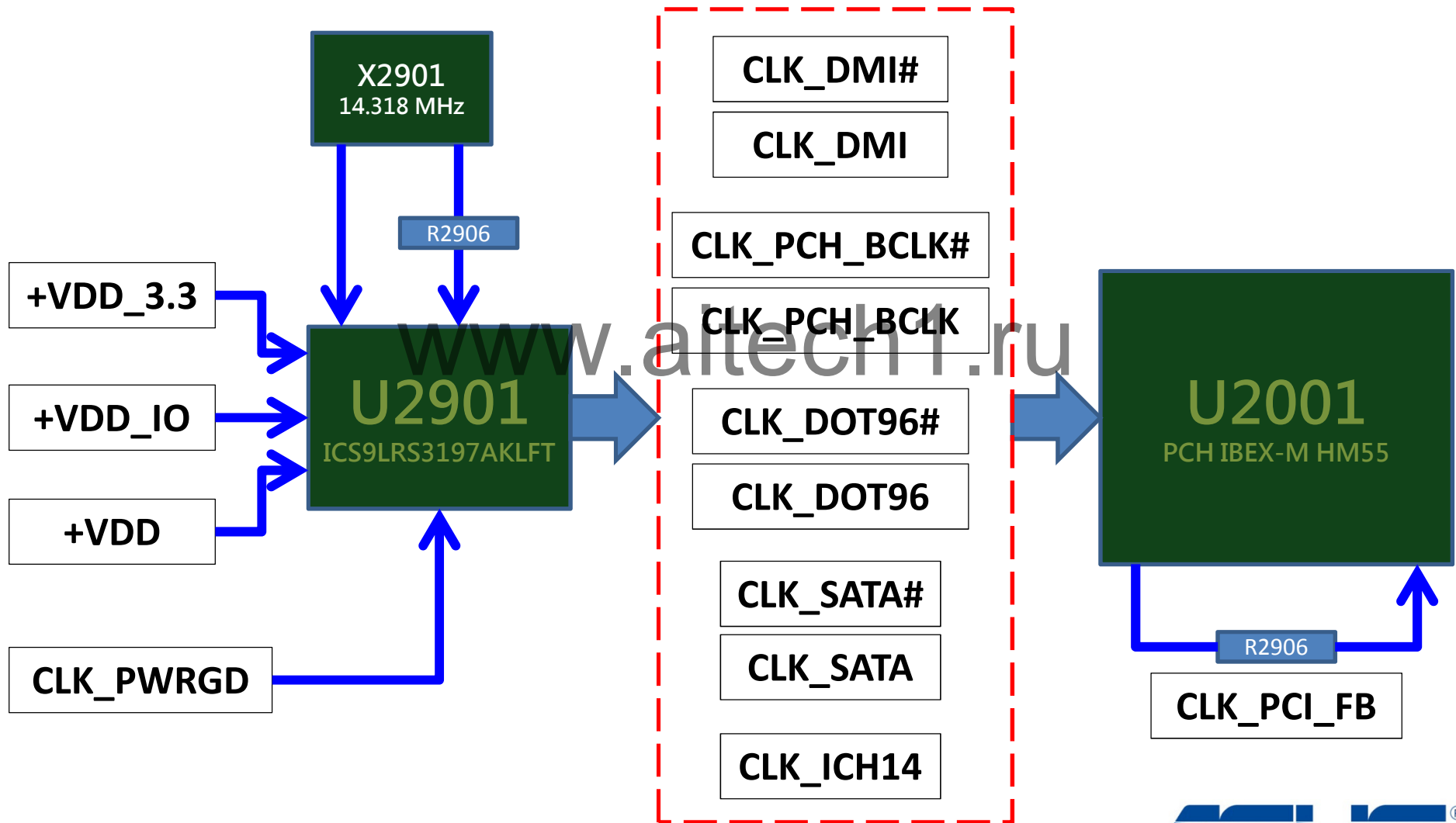
➤ Connection problems between PCH and CPU

Critical Power sources to PCH (2)



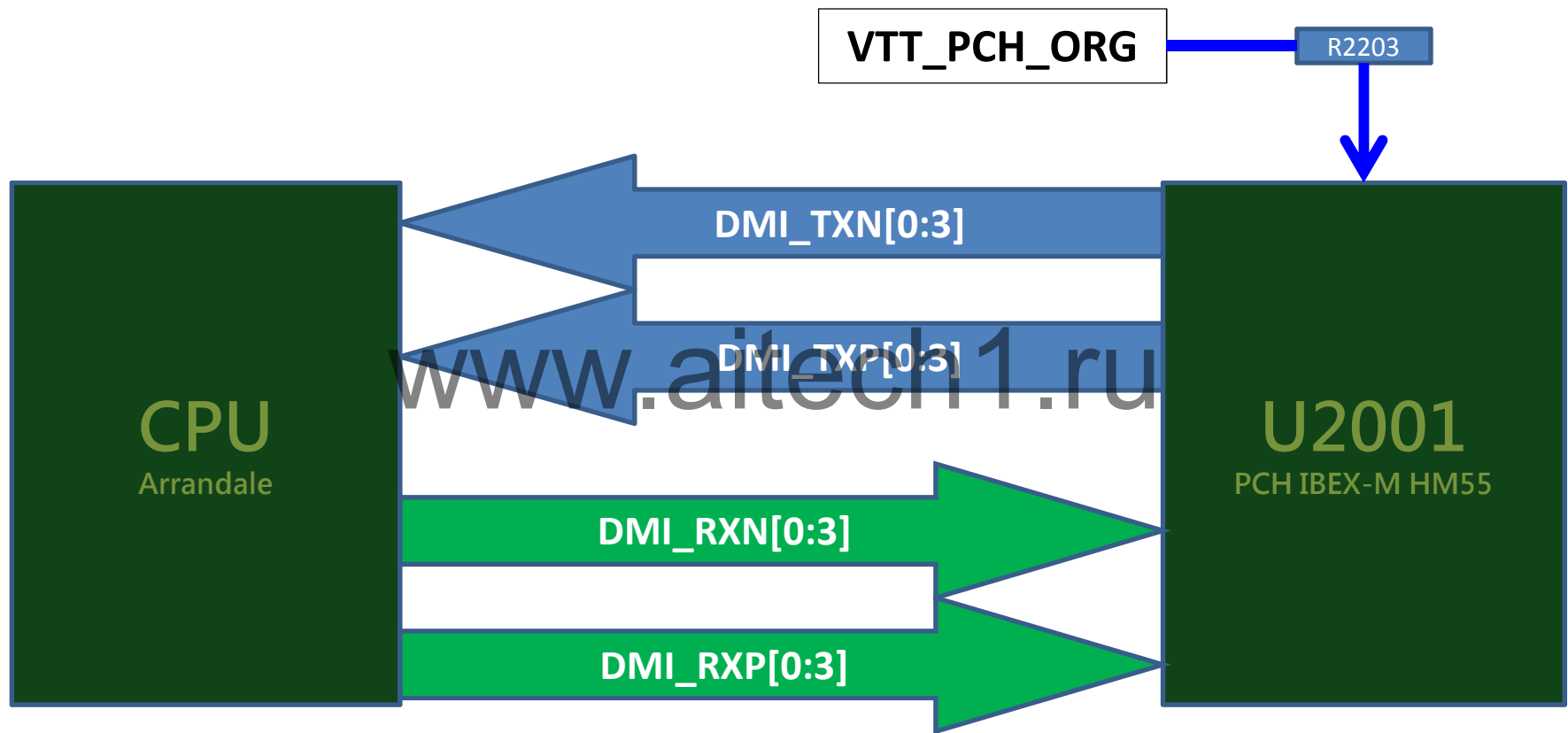
➤ Connection problems between PCH and CPU

Critical Clocks from clock generator to PCH



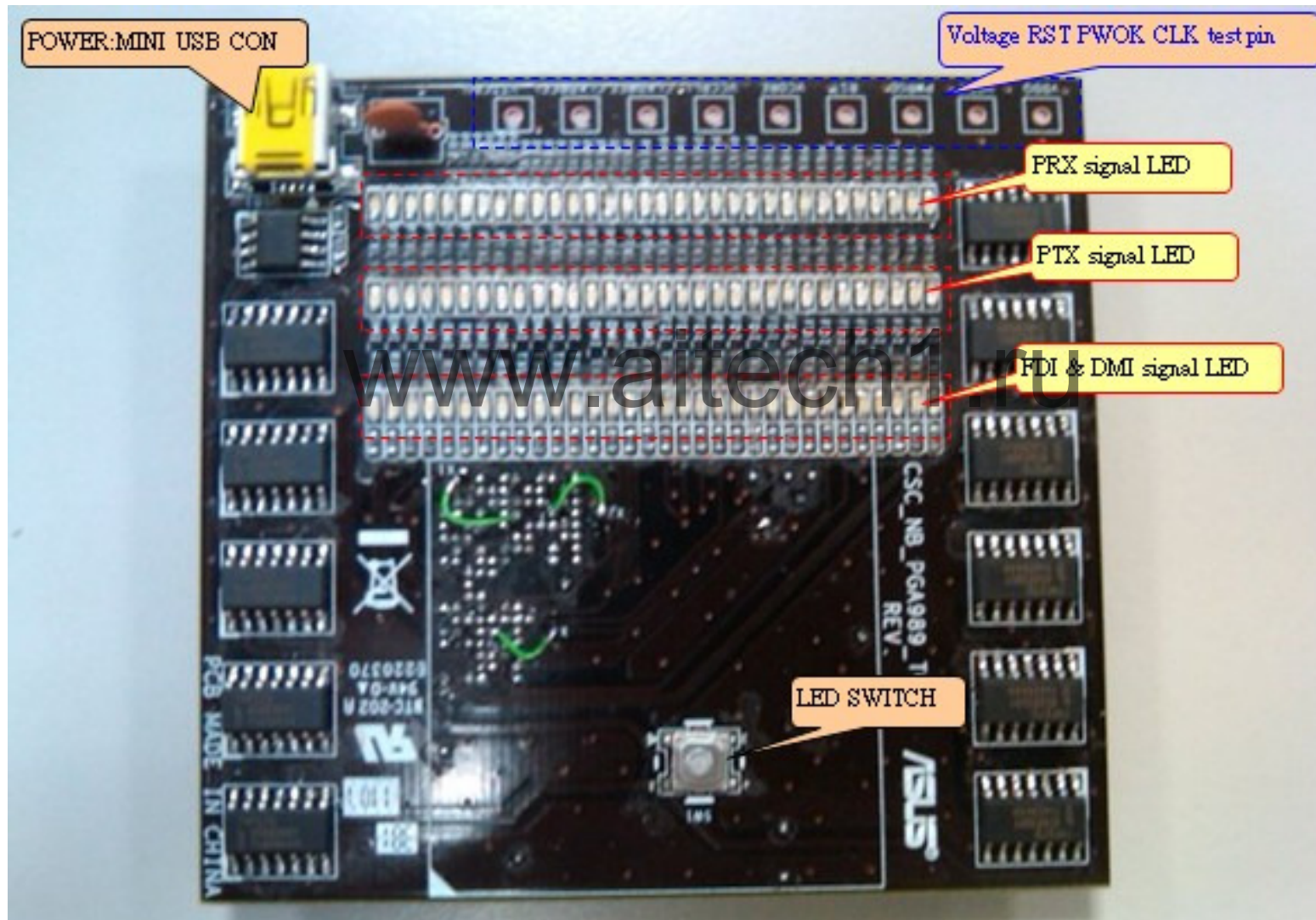
➤ Connection problems between PCH and CPU

Data Transmission pins between PCH & CPU



➤ Connection problems between CPU and RAM(s)

PGA989 CPU inspection Tool



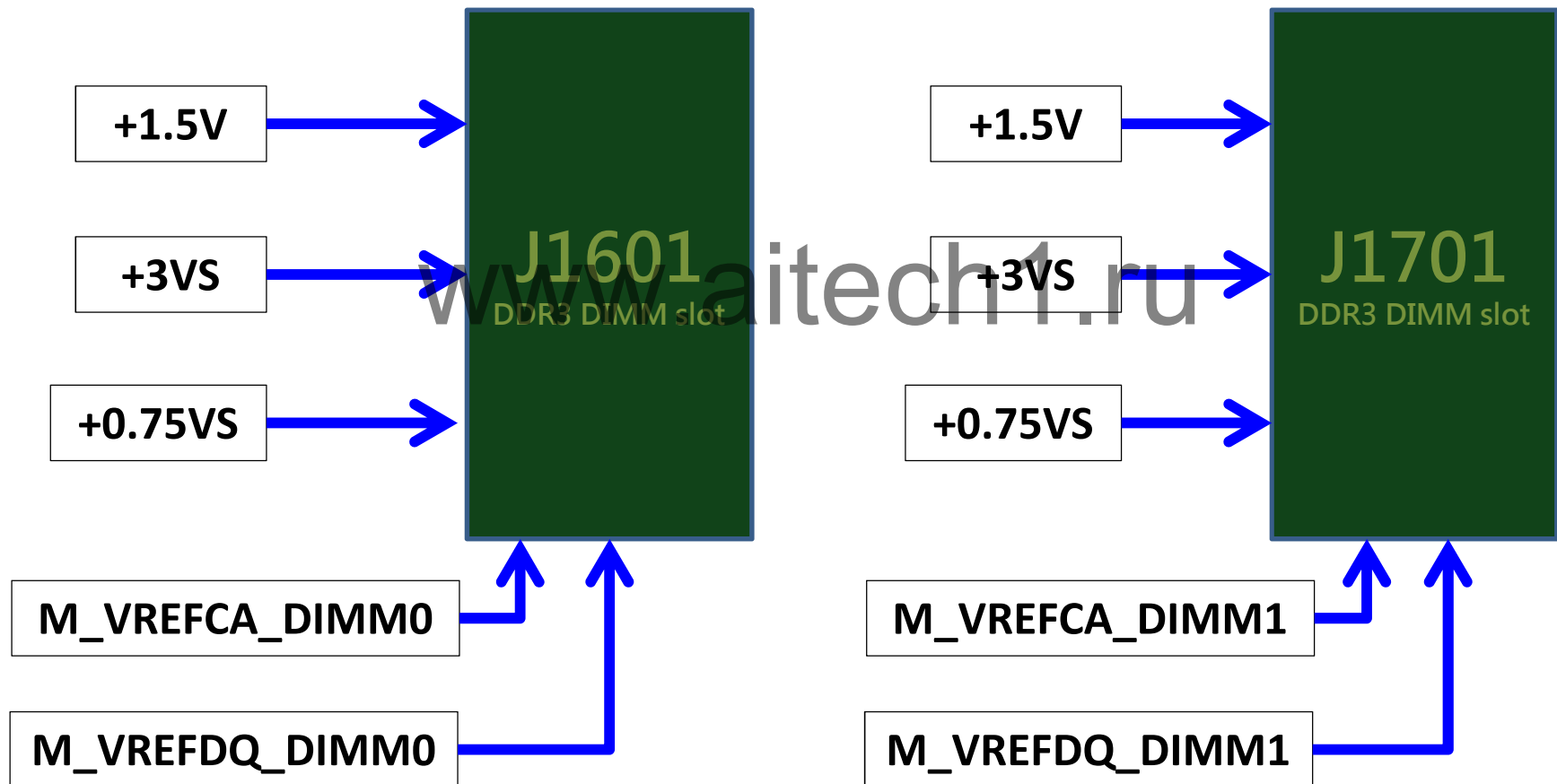
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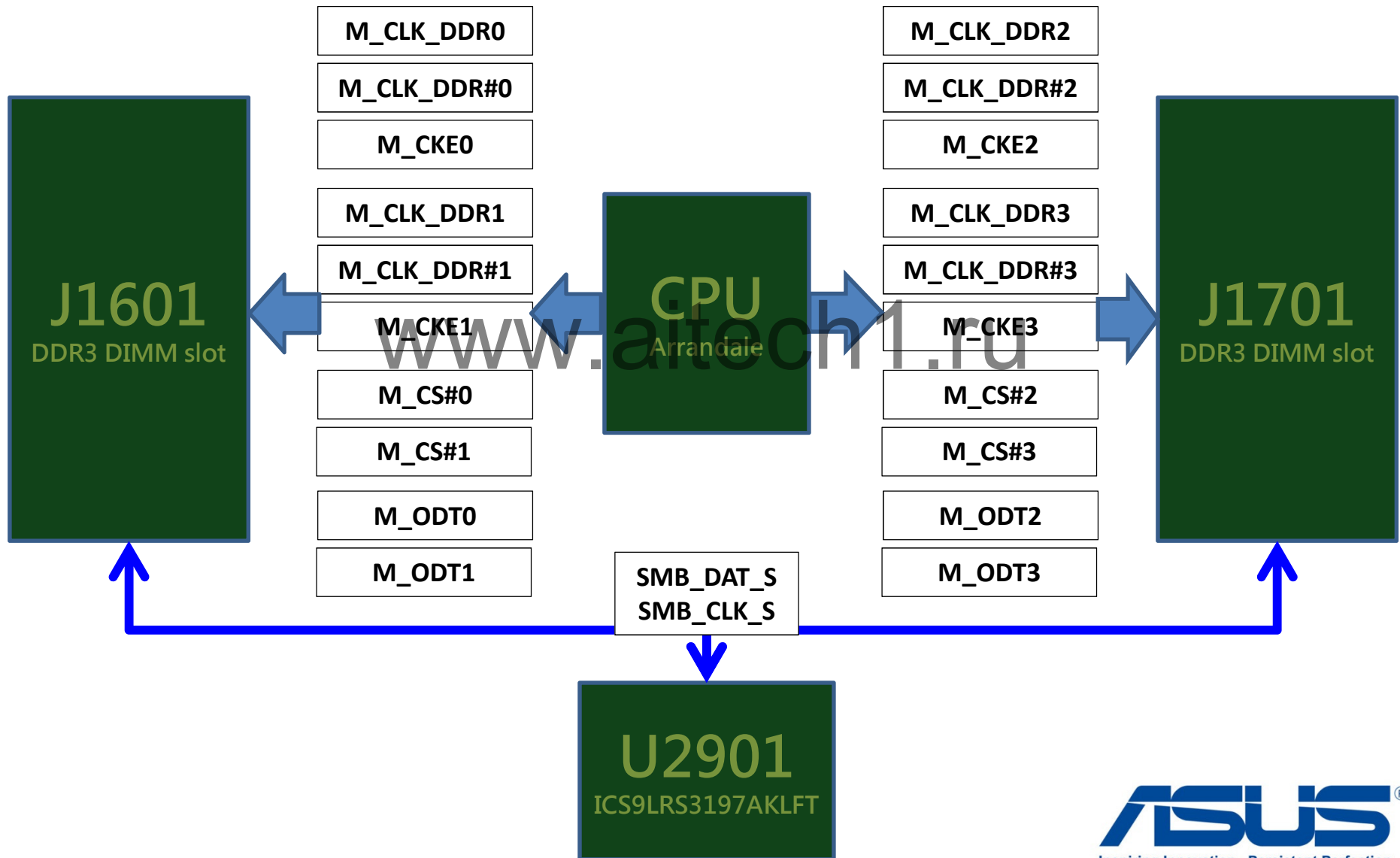
➤ Connection problems between CPU and RAM(s)

Critical Power sources to DDR3



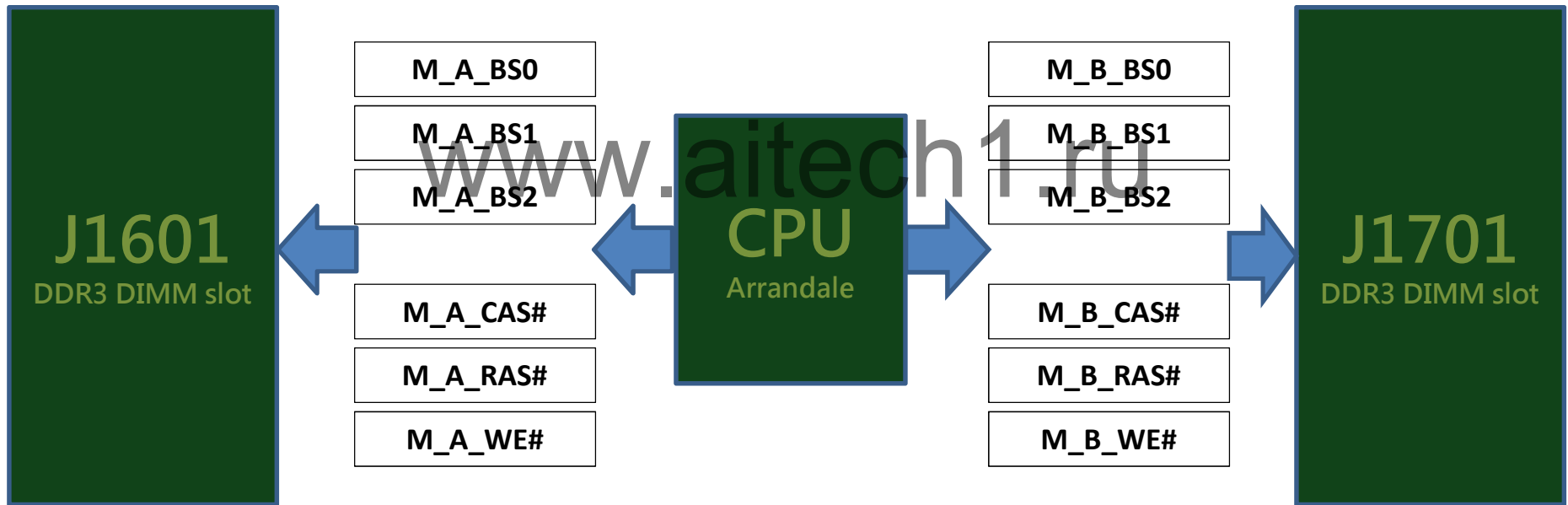
➤ Connection problems between CPU and RAM(s)

Critical Clocks and Control signals to DDR3 (1)



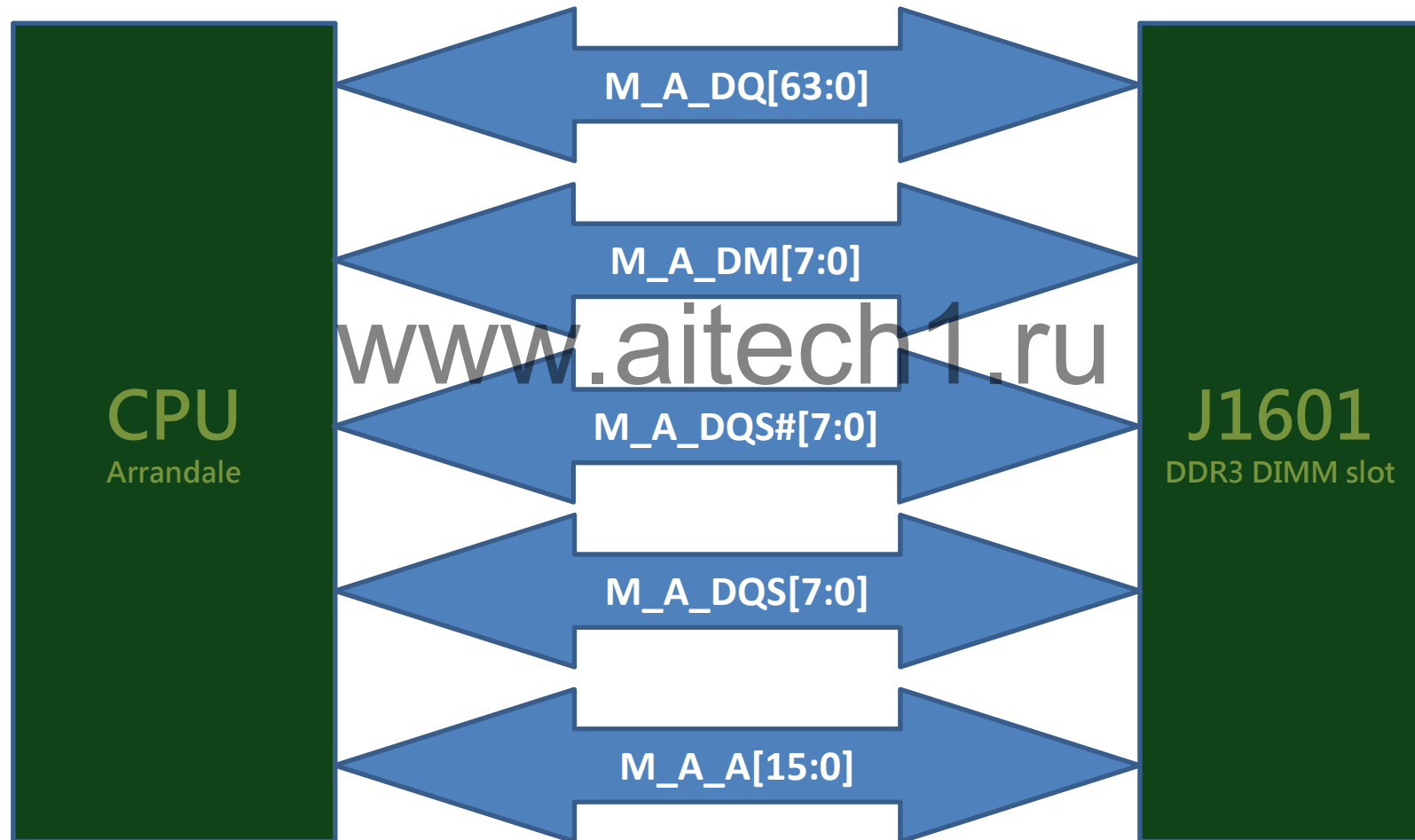
➤ Connection problems between CPU and RAM(s)

Critical Clocks and Control signals to DDR3 (2)



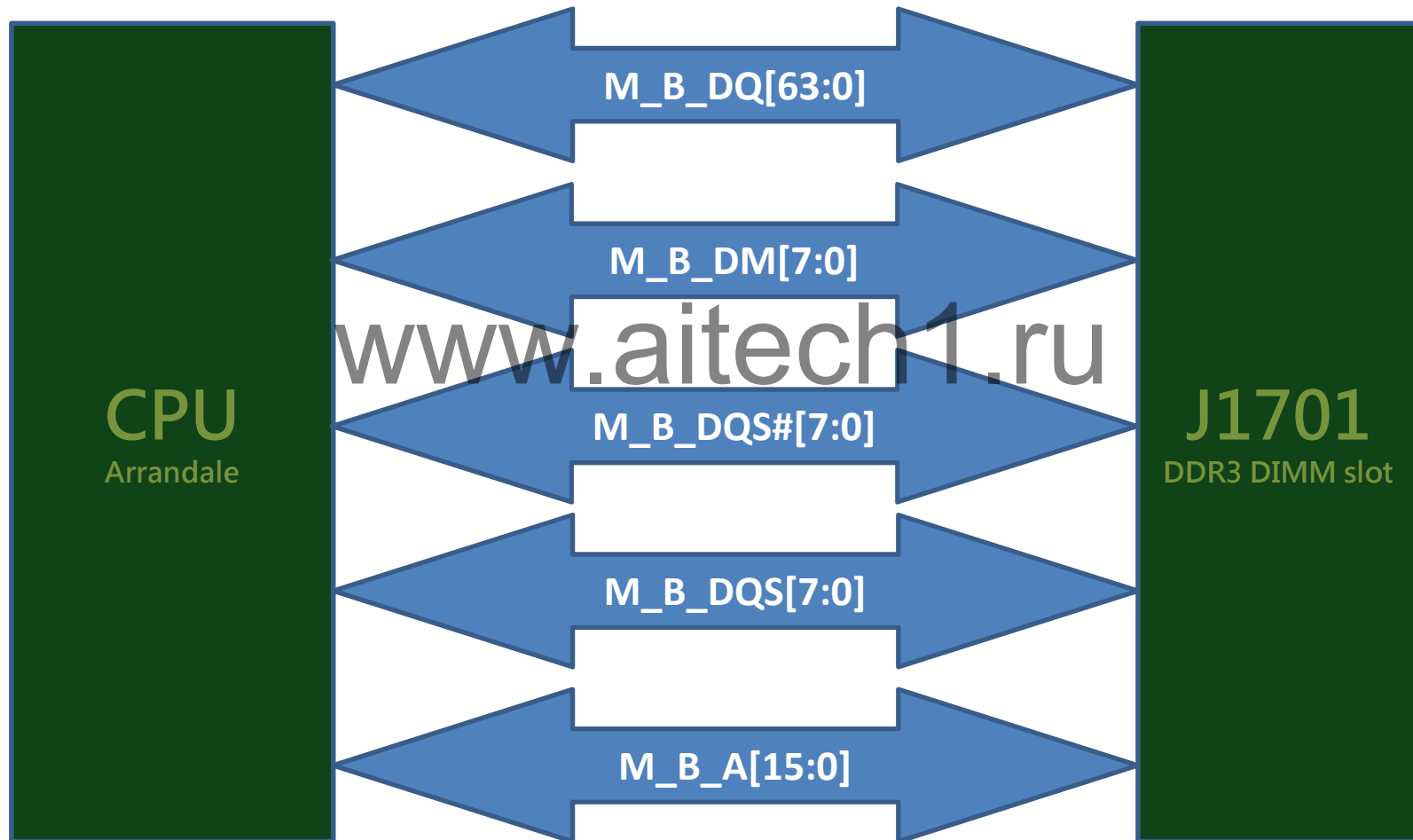
➤ Connection problems between CPU and RAM(s)

Data Transmission pins between CPU and DIMM0



➤ Connection problems between CPU and RAM(s)

Data Transmission pins between CPU and DIMM1



➤ Connection problems between CPU and RAM(s)

DDR3 inspection Tool

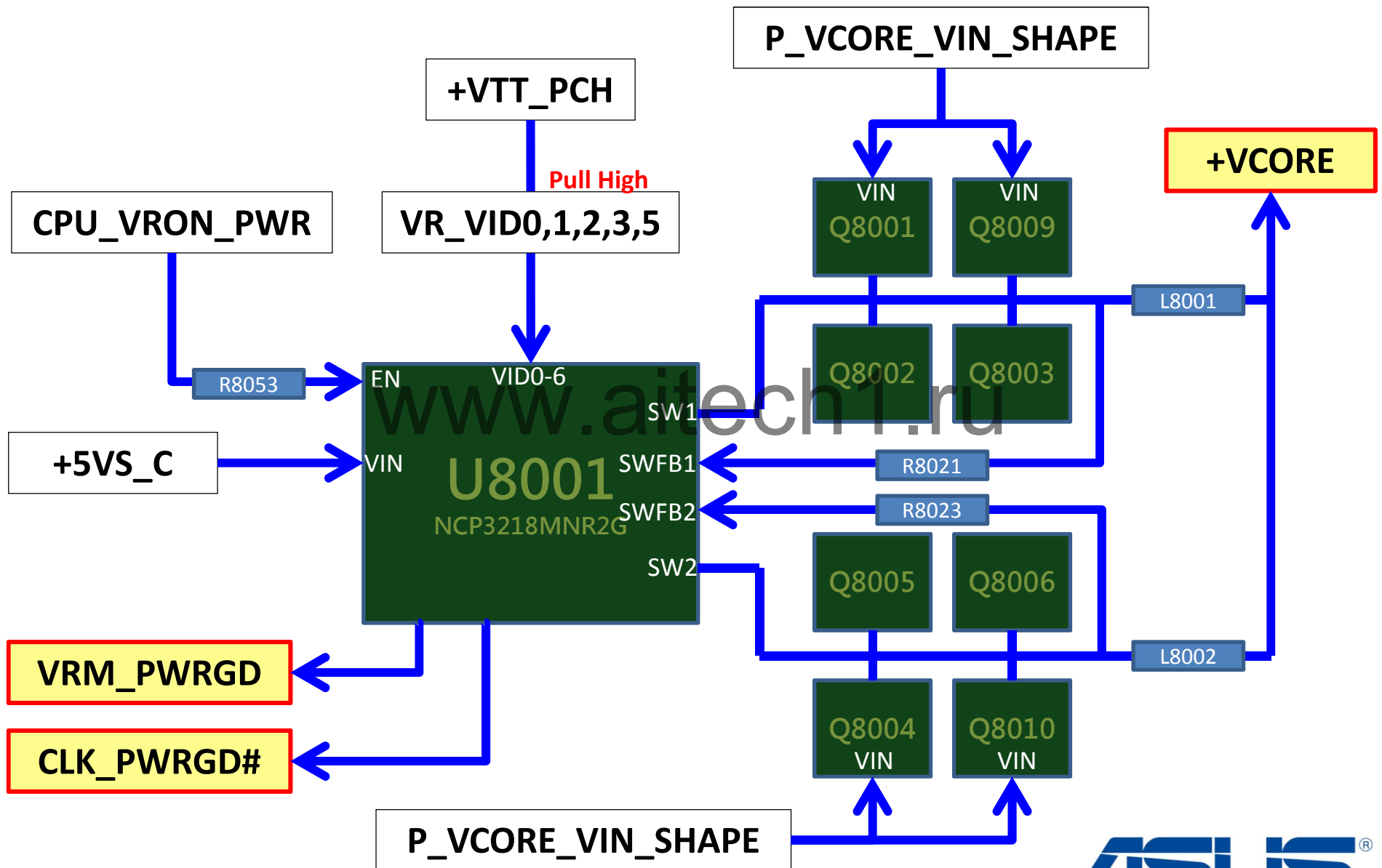


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➤ VCORE Problems



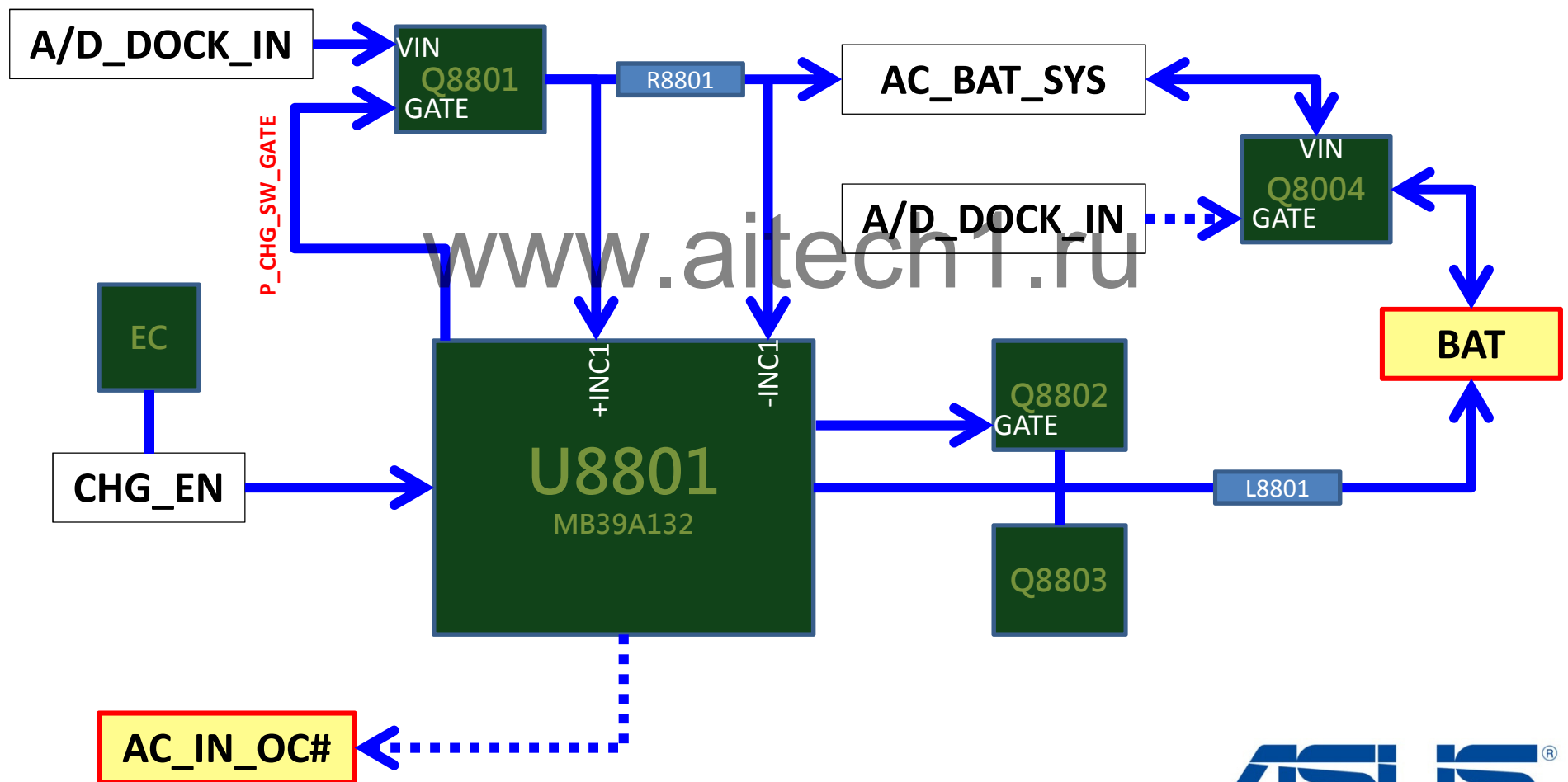
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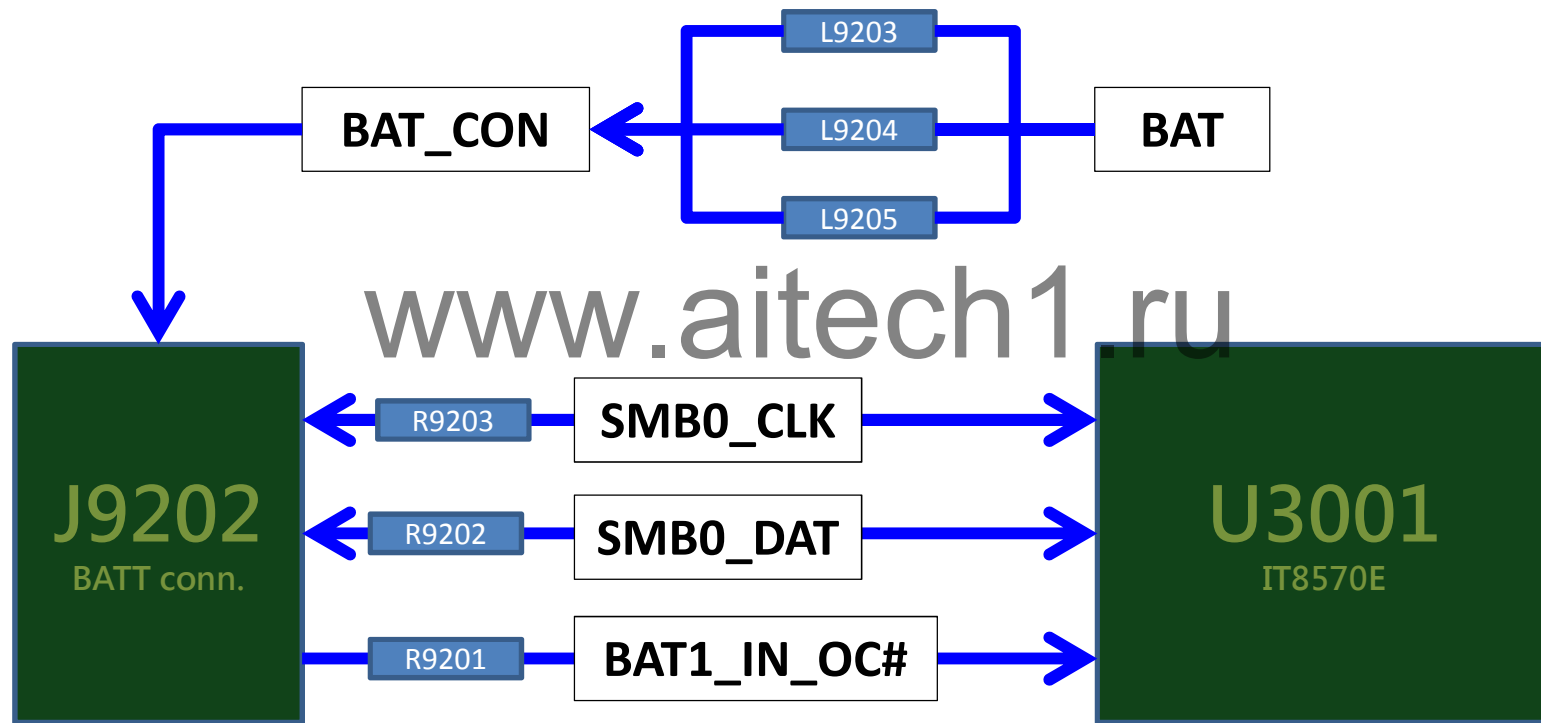
➤ Battery Charging Problems

Battery cannot be charged due to Power (BAT) problems



➤ Battery Charging Problems

Battery cannot be charged due to Signal detection problems

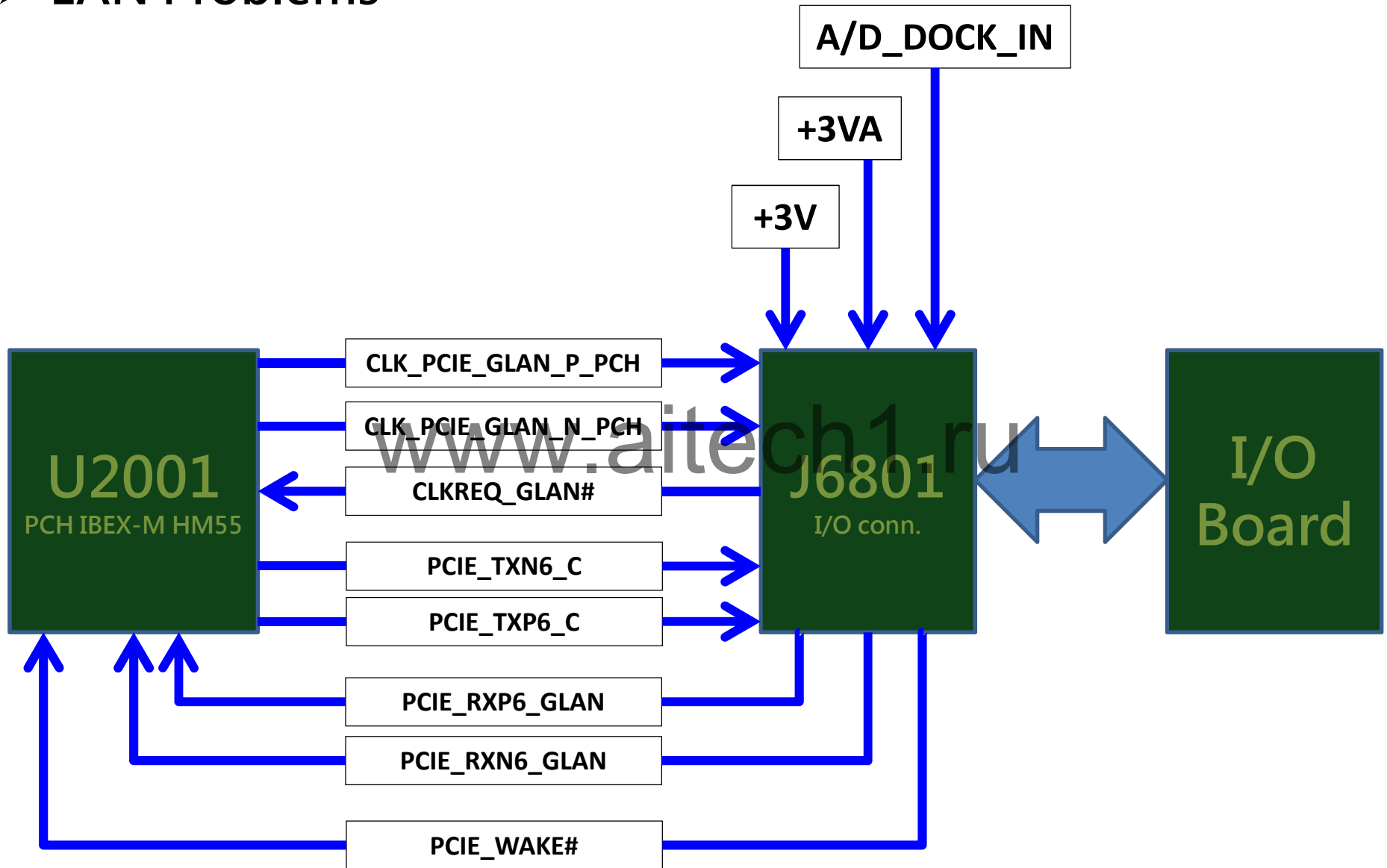


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➤ LAN Problems

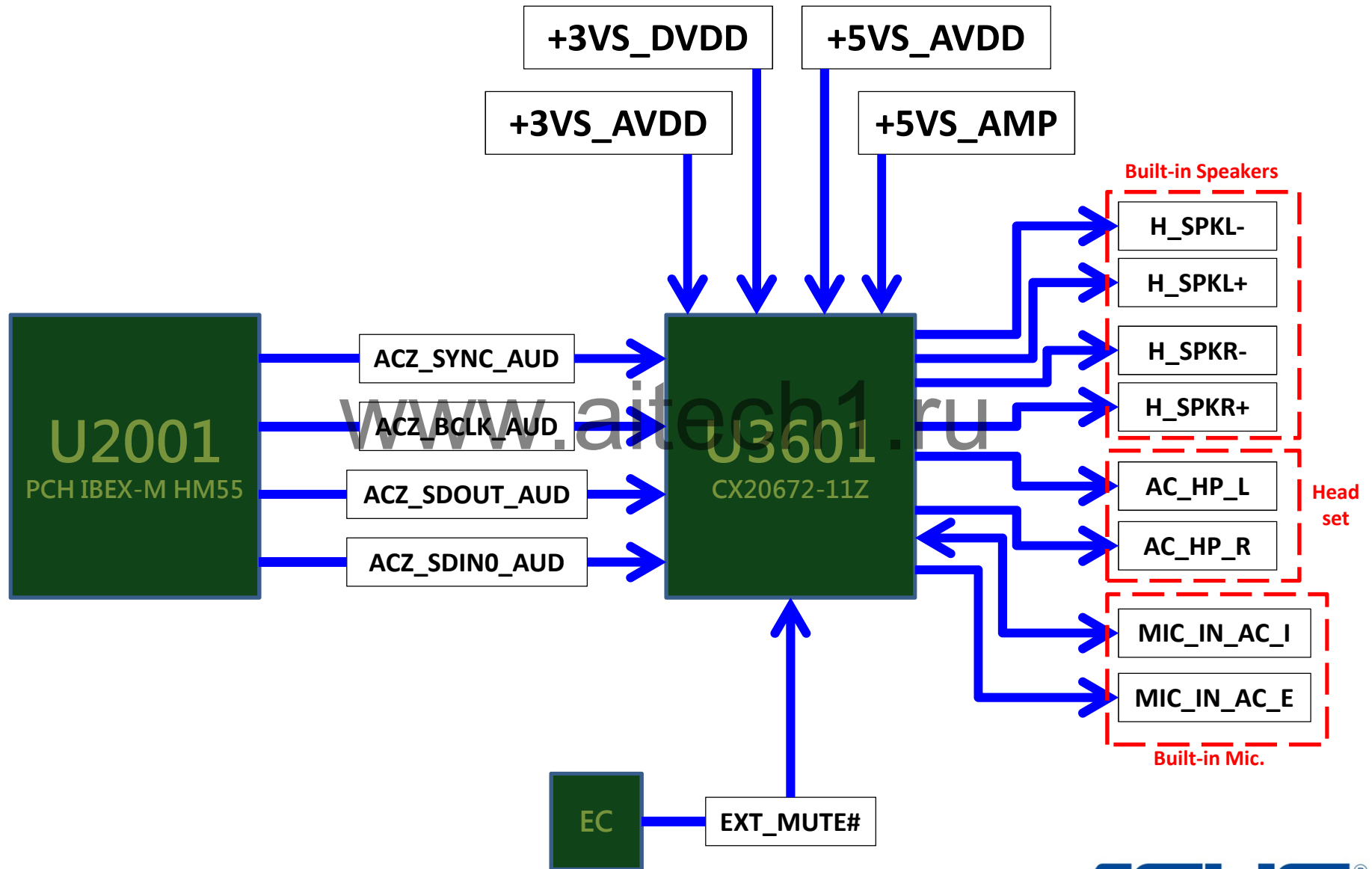


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➤ Audio Problems



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THANK YOU